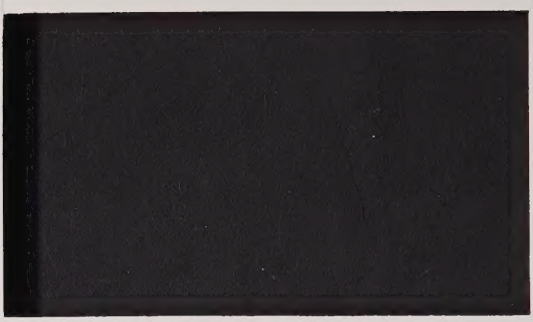
datum inc.

Timing Instrumentation



ME-10571

TECHNICAL MANUAL

MODEL 9300A 9012
TIME CODE
GENERATOR/TRANSLATOR
PART NO. 9300-7323

DATUM INC., TIMING DIVISION

1363 S. State College Blvd., Anaheim, Calif. 92806 - phone (714) 533-6333 twx (910) 592-1289

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MANUAL ADDENDUM

EQUIPMENT CONFIGURATION

The Model 9300 Time Code Generator/Translator (TCG/T) consists of a basic unit, to which optional features are added. Sections One through Five of this manual describe the basic 9300 TCG/T. Material pertaining to optional features is contained in Appendix B.

The Model 9300-7323 TCG/T contains the following options and/or modifications:

1. S/H/ REGISTER (Assembly 16989)

This logic, which is controlled from the I/O Control Logic (see following paragraph(s)) converts the data to three (3) 16 bit data words (see Appendix B for Word Format).

2. I/O CONTROL (Assembly 18180)

This logic controls the output data words as defined in the Word Format. I/O Control and data lines are on rear panel connector J5. See Drawing Number 809253 for typical In/Out connections.

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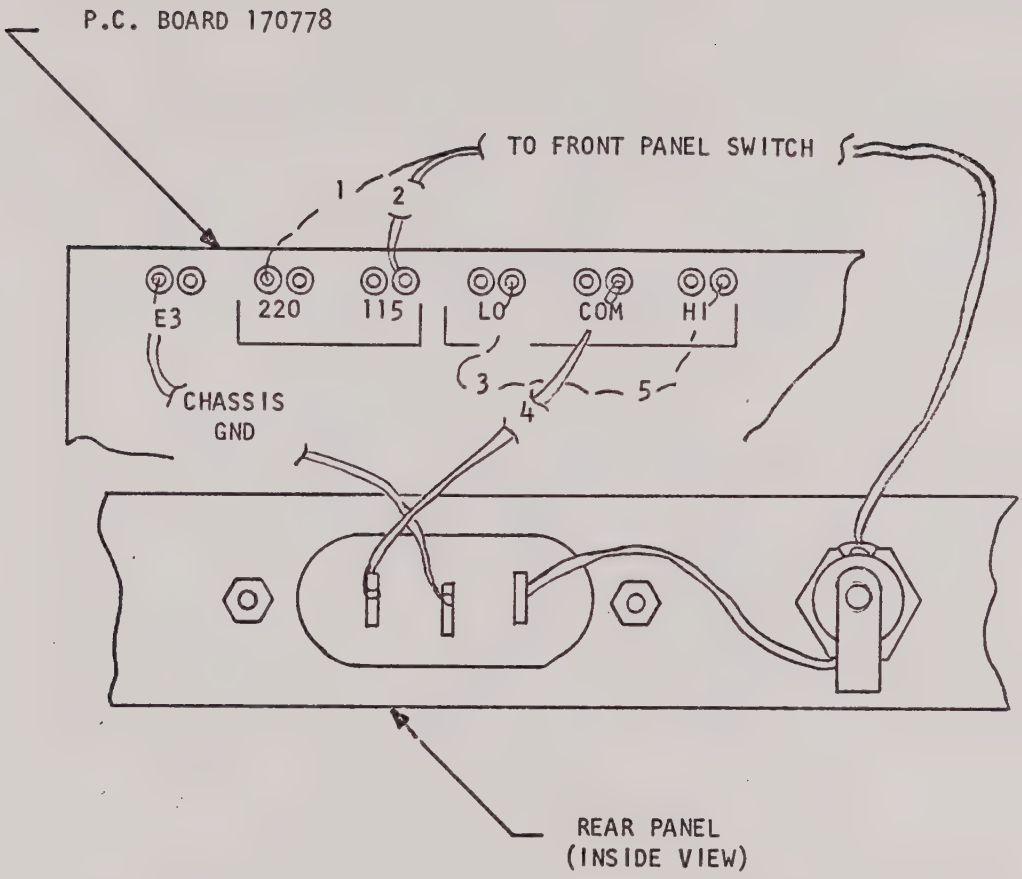
NOTE:

1. The Model 9300 is shipped for use with 115V AC operation unless identified for 220/230 VAC at AC power connector. See next page for changes to 220 VAC operation.



1. Jumper #1 For 220 VAC Operation
2. Jumper #2 For 115 VAC Operation
3. Jumper #3 For Lo Line Voltage
4. Jumper #4 For Normal Line Voltage
5. Jumper #5 For Hi Line Voltage

SECTION I
SYSTEM DESCRIPTION

1.1 The Model 9300 Time Code Generator/Translator is designed to perform two basic functions. First, the unit generates a time code in suitable form for recording on magnetic tapes or paper charts. Secondly, the unit is capable of reading the recorded time when played back from a magnetic tape or other sources. The standard format includes BCD seconds, minutes, hours and days only in both the generator and translator modes.

1.2 TIME CODE GENERATOR

As a Time Code Generator the Model 9300 develops a serial modulated time code, modulated to allow recording or magnetic tape or to allow convenient distribution to remote users. The NASA 36-Bit format is used so that the unit is compatible with many other existing facilities or other standard instrumentation equipment. Front panel controls allow the clock to be stopped, started or preset. Each digit of seconds, minutes, hours and days is settable to allow time-of-day or elapsed time operation. The basic clock accumulates time on a 24-hour basis and is accurately updated each second.

1.3 TIME CODE TRANSLATOR

When placed in the translate mode the unit will accept the NASA 36-Bit format either as generated in the Time Code Generator mode or as received from other sources. The unit automatically decodes the serial input code and provides a front panel display, serial pulse trains and optional digital outputs. Reading accuracy is better than 50 microseconds when reading in the forward playback mode.

A synchronization mode, selectable from the front panel, provides noise rejection. This feature allows the selection of "zero", "one," two," "four," "eight," or "infinite" time frames bypass if input errors are detected. This feature is most important when digital outputs are required, or tape search operation is desired. With "zero" selected each time frame is read. With one, two, four or eight selected, the unit is resynchronized only after the selected number of consecutive errored frames. With "infinite" selected,

the unit updates from the carrier only and disregards the coded information. The unit must be synchronized in one of the other bypass positions prior to selecting the "infinite" mode.

1.4 PHYSICAL

The Model 9300 is constructed in a 1-3/4" package, requiring minimum 19" rack mounting or offering easy handling for desk mounting. A decimal display located on the front panel, shows either generated time or translated time depending on mode of operation. All operating mode controls are mounted on the front panel. Each display digit is individually presettable with a single thumbwheel switch and a pushbutton for each digit.

The circuitry of the Model 9300 consists of TTL and DTL type integrated circuits. Each element is mounted in a modular socket for ease in maintainablility.

SECTION II
SPECIFICATIONS

2.1 INPUTS

2.1.1 J1 Code Input

a.	Format:	NASA 36-Bit (Control functions may be included in the code but are not recognized as valid data in the standard instrument.)
b.	Modulation Frequency:	1 kHz
c.	Modulation Ratio:	2:1 - 4:1
d.	Amplitude:	100 MV p-p to 10V p-p on the mark pulse.
e.	Input Z:	100K at 1 kHz
f.	Frequency Range:	25 Hz - 200 kHz
g.	Synchronization Accuracy	Less than ±50 microseconds

2.1.2 J6 AC Power

a.	Voltage Requirements:	115/220V AC ±10%
b.	Frequency:	48 - 420 Hz
c.	Power Requirements:	$\leq$75 watts

2.2 OUTPUTS

2.2.1 J2 NASA 36-Bit Modulated Code

(Note: This output is only available when operating in the GEN mode.)

a.	Carrier Frequency:	1 kHz sinewave
b.	Amplitude:	Adjustable from 0 to 10V p-p on the mark pulse.
c.	Modulation Ratio:	Adjustable from 2:1 through 6:1
d.	External Load:	$\geq$600 ohms

2.2.2 J3 Standard Pulse Rates

a. Rates:

1K pps	Pin 1
100 pps	Pin 2
10 pps	Pin 3
1 pps	Pin 4
GND	Pin 6

b. Duty Cycle: 80/20%

c. 1K pps: 50/50% (in translator mode)

d. On Time Edge: Negative

e. Output Levels: Logic "0" $\leq$ 0.4 VDC
Logic "1" $\geq$ 2.4 VDC

f. Source Impedance: DTL/TTL Compatible

2.2.3 J3 Bi-Level Five Rate Slow Code **(Optional)**

a. Format: DATUM Slow Code

b. Amplitude: Adjustable - 10V (maximum) on the "mark" pulse.

c. Source Impedance: 100 ohms

d. Pin 5 - CODE
Pin 6 - GND

2.2.4 J4 Parallel Outputs **(Optional)**

These outputs consist of milliseconds, seconds, minutes, hours and days BCD time data.

a. See Table 1 for pin assignments

b. BCD outputs are TTL positive true logic. Logic "0" $\leq$ 0.4 VDC
Logic "1" $\geq$ 2.4 VDC

c. Sample Time pulse is normally true-pulsing to a Logic "0" (GND) for approximately 2 microseconds at update time (1K pps rate).

d. See Section III, paragraph 3.7, for Tape Search Operation.

2.2.5 J5 Parallel Outputs **(Optional)**

a. See Table II for pin assignments.

b. 32-Bit BCD time-of-year (S, M, H, D)

c. Output Levels:	Logic "0" $\leq$0.4 VDC
	Logic "1" $\geq$2.4 VDC
d. Source Impedance:	DTL/TTL Compatible
e. Sample Time:	Approximately 2 μsec pulse to a logic "0" at update time (1 pps rate).

2.3 Time Base

a. Type:	Oven Controlled Oscillator
b. Frequency:	1MHz
c. Stability:	$\pm 5 X 10^{-6}$

2.4 Environment

a. Temperature:	$0^{o}C$ to $+50^{o}C$
b. Humidity:	Up to 95% relative

2.5 Physical

a. Panel Height:	1-3/4 inches
b. Chassis Width:	17 inches
c. Chassis Depth:	18 inches

TABLE 1

PIN ASSIGNMENTS

J4 Parallel Outputs (Binary Coded Decimal) (Optional)

Pin	Term	Pin	Term
1	mS1	26	M40
2	mS2	27	H1
3	mS4	28	H2
4	mS8	29	H4
5	mS10	30	H8
6	mS20	31	H10
7	mS40	32	H20
8	mS80	33	D1
9	mS100	34	D2
10	mS200	35	D4
11	mS400	36	D8
12	mS800	37	D10
13	S1	38	D20
14	S2	39	D40
15	S4	40	D80
16	S8	41	D100
17	S10	42	D200
18	S20	43	D400
19	S40	44	D800
20	M1	45	FWD*
21	M2	46	FRP
22	M4	47	GO
23	M8	48	SAMPLE TIME
24	M10	49	$\overline{\text{SEARCH}}$
25	M20	50	GROUND

TABLE II

PIN ASSIGNMENTS

J5 Parallel Outputs (Binary Coded Decimal) (Optional)

Pin	Term	Pin	Term
1	S1	19	H10
2	S2	20	H20
3	S4	21	D1
4	S8	22	D2
5	S10	23	D4
6	S20	24	D8
7	S40	25	D10
8	M1	26	D20
9	M2	27	D40
10	M4	28	D80
11	M8	29	D100
12	M10	30	D200
13	M20	31	D400
14	M40	32	D800
15	H1	33	NOT USED
16	H2	34	SAMPLE TIME
17	H4	35	GROUND
18	H8	36	GROUND

SECTION III
OPERATING PROCEDURE

3.1 GENERATE MODE

a. Apply AC power to J6.

b. Turn on instrument by moving the PWR switch, located on the front panel, to the ON position.

c. Rotate the MODE switch to the HOLD position. (Display should be stationary.)

d. Preset the time of day using the following procedure:

1. Start with the least significant digit (unit seconds) and in progression finish with hundreds of days.

2. Select the number to be preset into each decade with the PRESET thumbwheel switch.

3. Press the pushbutton under each decade to enter the PRESET number into the output register.

e. Rotate the MODE switch to the GEN position. At the preset start time, press the START pushbutton.

f. The display will now update at a 1 pps rate and all outputs will be available on their respective output connectors.

3.2 TRANSLATE MODE

a. Apply power as in steps a and b of the GENERATE MODE procedure.

b. Place a standard 1 kHz modulated NASA 36-Bit code on BNC connector J1 located on the rear of the unit. It does not matter if the code format has been modified to remove the control functions as this portion of the time code is not used for decoding purposes in the 9300. (See 9300 specifications for modulation ratio, frequency range and amplitude requirements.)

c. Rotate the MODE switch to the TRANS position.

d. Place the FWD/REV switch to the FWD position.

e. After allowing approximately one minute after turn-on for the AGC to settle, the 9300 will automatically synchronize to the input time code.

NASA Basic

3.3 BY-PASS OPERATION (See also paragraph 3.12)

a. Select TRANS. The 9300 will respond to each time frame of the input code. Any degradation of the input code may cause an erroneous reading on the 9300 Time Code Generator-Reader.

b. Select 4. The 9300 will sync to the input code, then automatically lock out its own sync circuits and just monitor the input code for time differences. Frame errors are counted; however, the 9300 synchronization is not disturbed unless four consecutive errored frames are counted. If frame errors are separated by a valid frame, the error counter is reset to zero; therefore, resynchronization can only take place on the fifth frame after counting four consecutive errored frames. This mode can be extremely useful when input time code is noisy or being derived from a poor or spliced tape.

c. oo BY-PASS. Note: Prior to selecting this position, the 9300 must be synchronized in either the TRANS, 1, 2, 4, or 8 position. After synchronization, rotate the MODE switch to the oo Bypass position. Once in this mode, all synchronizing functions are locked out and the 9300 will act as an elapsed time generator updating on the carrier rate of the input code.

3.4 DIRECTION CONTROL

The 9300 is provided with manual direction control and is operated by means of a front panel mounted toggle switch, INPUT FWD/REV. For forward operation place this switch in the FWD position. For reverse translation, place the switch in the REV direction.

3.5 INPUT CODE POLARITY CONTROL

The 9300 includes provisions to compensate for inverted polarity input codes. This is done with a front panel mounted toggle switch, INPUT +/-. For normal operation, this switch should be placed in the (+) position. For inverted polarity input codes, place the switch in the (-) position.

3.6 INTERNAL FILTER CONTROL

An internal 3 kHz low pass filter has been provided in the 9300, for use in playback (X1 speed ratio) operation. To activate the filter, place the front panel mounted FILTER IN/OUT switch to the IN position.

3.7 TAPE SEARCH OPERATION (Optional)

a. Connect the 9300 to the Tape Search unit as described in the Tape Search unit instruction manual.

b. Insure that the FWD/REV switch is in the FWD position and that the FILTER switch is in the IN position.

c. A logic "1" on Pin 45 of J4 will program the 9300 for forward operation, a logic "0", for reverse operation.

d. A logic "1" on Pin 49 of J4 will activate the low pass filter, a logic "0" will de-activate the filter.

e. A logic "0" Pin 47 of J4 will inhibit updating of the 9300.

3.8 5 RATE SLOW CODE (Optional)

The PRESET thumbwheel switch serves a dual function when the Slow Code option is installed. In addition to serving in the PRESET function, positions "1" through "5" select the desired frame period (see slow code drawing in Section V). Position "0" de-activates the Slow Code circuitry.

3.9 INPUT CODE SELECT (Optional)

Rotate the MODE A/B/E switch to program the 9300 to accept either IRIG A, IRIG B or IRIG E as the input code.

3.10 ADVANCE/RETARD (Optional)

a. Preset and start the generator as described in paragraph 3.1 above.

b. Sync an oscilloscope on the "on-time" edge of an external reference pulse (1 PPS).

c. Observe the "on-time" edge of the equivalent local pulse rate. If the local pulse appears to the right of the reference, the 9300 is "late." If the local pulse occurs to the left, the 9300 is "early."

d. Select the greatest Advance/Retard rate (refer to SWITCH & CONTROL LOGIC (11) drawing for rate identification) which will not overcorrect for the offset in one second. For example: for an offset of 5 milliseconds, the proper rate would be 1 millisecond/second, as 10 milliseconds/sec would overcorrect.

e. If the logic pulse is "early," press the RET pushbutton. If the local pulse is "late," press the ADV pushbutton. Observe that the local pulse appears to move toward the reference pulse.

f. When the local pulse is within one second correction capability, select the next slowest correction rate.

g. Continue in this manner until the local pulse is alligned to within the maximum resolution of the Advance/Retard circuit.

3.11 EXTERNAL START (Optional)

a. Connect the external start pulse (1 PPS) to the INPUT BNC on the front panel. Place the WWV/DC switch in the appropriate position in accordance with the type signal to be used. Observe that the TICK indicator blinks at a 1 PPS rate.

b. If a WWV "tick" is being used, rotate the LEVEL control to the maximum counter-clockwise position. Adjust this potentiometer clockwise to obtain a steady blinking of the TICK indicator. Setting the control more clockwise than required to obtain a reliable indication may result in an unreliable start.

c. Preset the generator as described in steps 3.1. Rotate the MODE switch to the GEN position.

d. After the "Tick" which occurs one second prior to the preset start time, press the ARM pushbutton. The ARMED indicator will light.

e. The next "Tick Pulse" will start the generator.

3.12 DETAILED BY-PASS OPERATION

When this switch is set to "0" (TRANSLATE), the instrument monitors the input code and responds to each time frame of the input code. If the coded input is erroneous, the unit outputs the incorrect input value on both the visual display and the optional BCD output. However, the ERROR indicator is enabled (because a difference exists between the input and internal time values). This error status will remain until a subsequent code frame is input which is in agreement with the internal time value.

When this switch is set to "4", the instrument monitors the input code and if one or more frames are in error (up to 4), continues to properly update the displayed and BCD outputs by utilizing the 1 kHz carrier of the time code. Two (2) conditions affecting the ERROR indicator are as follows:

a. Less than four (4) consecutive 'erroneous' frames. The ERROR indicator is energized as long as a difference in time value exists between the input code and the internal time registers. At the end of a frame received in agreement with the internal time value, the ERROR indicator is de-energized.

b. Four (4) or more consecutive 'erroneous' frames.

   The ERROR indicator is energized as long as a difference in time value exists between the input code and the internal time registers. During the fifth consecutive frame, the time value

of the input code is entered into the internal time register. If the sixth consecutive frame of the input agrees with the updated time value in the internal time register, the ERROR indicator is de-energized at the end of this frame. However, if the sixth frame of the input code does NOT agree with the updated time value in the internal register, the input code value is again entered into the internal register and the next frame is again examined for agreement with the 'new' time value. The ERROR indicator remains energized and each subsequent frame time value is entered until time value agreement is found.

When the switch is set to "∝" (infinity), the instrument acts simply as an elapsed time generator, updated from its last time value by the carrier input. The ERROR indicator is energized when a difference in time value exists between the input time code and the internal time register and is de-energized at the end of the first frame found to be in agreement. Entering of input code time value(s) is inhibited whenever the switch is in the "∝" position.

Thus, the ERROR indicator is energized whenever (irrespective of switch position) a time value difference is detected between the code and the internal time register. Further, this status is de-energized at the end of the first subsequent code frame time value found in agreement with the internal time register. Therefore, the effect of the switch positions is to allow entering (jamming) of the input time code value into the internal time register under the following conditions:

a. "0" - each frame
b. "1" - the frame following a detected 'errored' frame
c. "2" - the frame following two (2) consecutive detected 'errored' frames
d. "4" - the frame following four (4) consecutive detected 'errored' frames
e. "8" - the frame following eight (8) consecutive detected 'errored' frames
f. "∝" - never

Finally, from the above examples, it may be discerned that the 'meaning' of the energized state of the ERROR indicator is that a difference in time value exists between the input code time value and the internal register time value and that the de-energized state of this status means there is no detected difference in these values.

SECTION IV
ADJUSTMENTS

The following is a list of adjustments which are basic to the 9300 Time Code Generator/Reader and includes those assemblies which are basic options. In the case of "Potentiometers," they are set at the factory to a nominal setting as indicated in ( ). However, the user should refer to the top assembly drawing for the location of these variables and adjust them for users specific requirements.

1. SINEWAVE SHAPER/MODULATOR ASSEMBLY
   a. R17 Level Adjustment. Range 0 to 10V peak to peak on the mark amplitude of the output code (3V p-p).

   b. R15 Modulation Ratio Adjustment. Range 2:1 - 4:1 mark to space ratio on the output code (3:1).

   c. R7 Phase Adjustment. Sets the phase of the carrier frequency so there is no discontinuity when amplitude modulation takes place.

2. POWER SUPPLY ASSEMBLY
   a. R10 adjusts the output level of the +5 volt regulator. Should be set to +5V ±2%.

3. SLOW CODE ASSEMBLY (Optional)
   a. R12 adjusts the output level (+6V mark amplitude)

SECTION V

THEORY OF OPERATION

5.1 LOGIC DESCRIPTION AND USE

The 9300 is depicted by several drawings. One of these is the top assembly drawing which shows the physical location of the assemblies that are contained within the instrument. This print should be used to locate connectors on the rear panel and for quick reference to the physical location of any of the assemblies or controls.

In the title block of each logic print is a circled number. For instance, the IRIG basic print (Minor Time) has circled number (8) in the title block. The IRIG basic print (Major Time) has circled number (9). The LED display has circled (12) in the title block. Except for terms originating within the drawing being studied, this reference number will precede each term, showing the sheet of logic upon which it originated. To use these numbers. simply observe the term, look at the term reference number in front of the term, then select the print that has this reference number in the title block. This print will show the point of origin of the term you are trying to find. This provides a convenient means of getting back and forth from various pages of these logics.

Each time a term reference number will refer you back to the source of that signal. In each of the logics there will be a number such as A4, A8, A11, etc. These number refer to the physical location on this assembly for that particular integrated-circuit element. In order to determine a physical location of an integrated circuit, one would merely refer to the top assembly drawing. In the lower left-hand corner of this drawing, each assembly contained within the instrument is listed, prefixed with a code letter, (ABC etc.) then, by referencing the mechanical view of the top of the instrument, look for the board labeled with that code letter. Examine the board until the desired integrated circuit is located.

All references in this discussion will be based on the circled term reference numbers located in the title blocks of all logic prints. The reader should be familiar with the above before preceeding.

5.2 GENERAL

The Model 9300 is both a time generator and a time translator. A time generator is a device which takes a referenced frequency and divides it so as to accumulate or "count" time intervals. A time translator is a device which requires a serial coded input and "decodes," or "translates" this input to some other form, usually parallel time data.

In order to better understand the logic organization of the 9300, let's first review the basic configuration of typical timing units.

Figure 5-1 shows a simplified diagram of a typical Time Code Generator. The significant sections of a Time Code Generator are:

a. Frequency Source - Usually a crystal-controlled oscillator.

b. Minor Time Counters - The purpose of these counters is to develop scan terms and rates required to develop the serial code format or to be used for parallel outputs. They also supply a 1-pps signal that is used to update the Major Time Accumulator.

c. Major Time Accumulator - This section is a counter whose function is to store the time-of-year data. It is incremented by the 1 pps clock output of the frequency dividers. Its outputs are buffered and used for parallel outputs or they are scanned by the encoder and outputted in a serial format.

d. Counter Control - This section synchronizes the time accumulator and includes switches to select and enter the time-of-day into the Major Time Accumulator.

e. Parallel-to-Serial Converter - This section consists of scan gates that serialize the contents of the accumulator into a continous pulse train.

TYPICAL TIME CODE GENERATOR

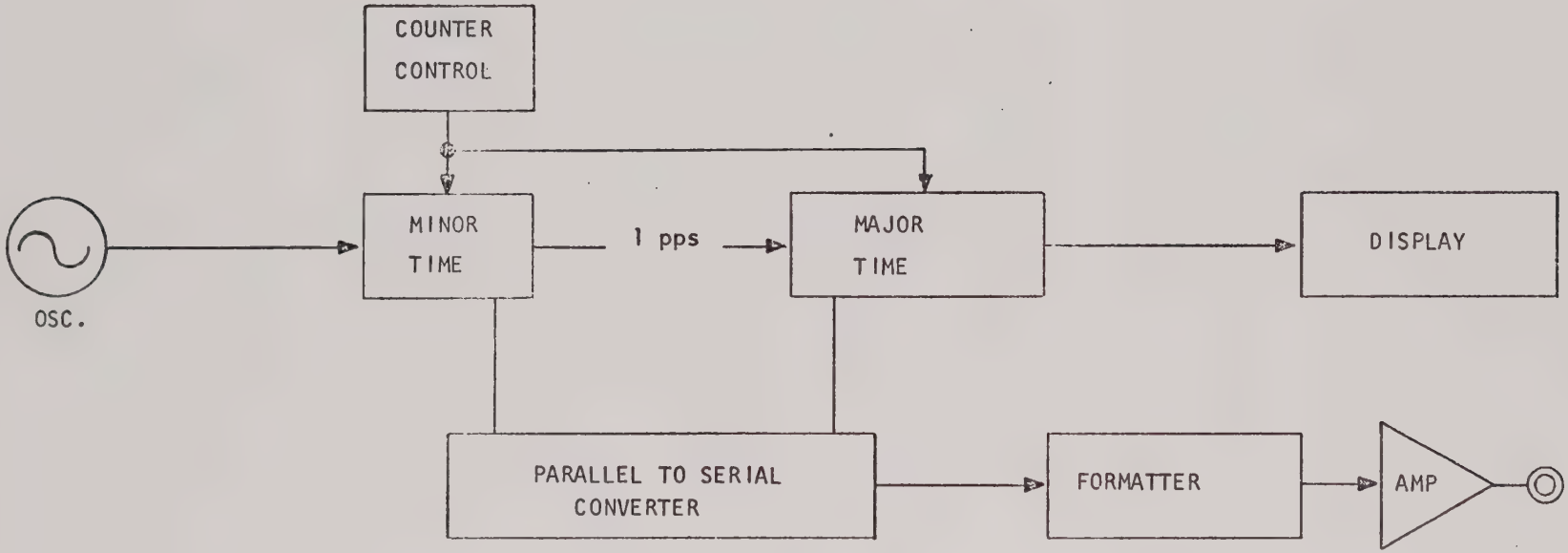


FIGURE 5-1

f. Formatter - This section uses pulse rates from the minor time counter to obtain the pulse widths and index pulses required to provide the format defined by the type of time code being generated. This format is then usually combined with a sinewave to provide an amplitude-modulated signal.

g. Output Amplifier - This section provides the required output drive and signal levels of the formatter output.

h. Display - This section interfaces the generator with the operator.

Figure 5-2 shows a simplified diagram of a typical Time Code Translator. The significant points to a Time Translator are:

a. Input Amplifier - Usually this is an AGC type amplifier. Its function is to provide a constant amplitude signal to the decode and detection circuitry.

b. Serial to Parallel Converter - This is the heart of the unit. Its function is to detect digital data in the input format and assign it to storage in the time accumulator. This portion contains the necessary circuits to synchronize the frequency dividers.

c. Frequency Dividers - These counters divide the carrier frequency. Once synchronized by the decoding circuitry in the serial-to-parallel section, this counter provides the terms necessary to index the digital data contained in the input code. This allows the locating of each code bit and the proper assignment to accumulator storage. Also important, they provide a 1 pps signal to update the Time Accumulator.

d. Time Accumulator - This counter stores the value being read from the input code. It is updated with the 1 pps signal from the frequency dividers and is permuted to count in the format of the input time code (usually seconds, minutes, and hours). Day-of-year may sometimes be provided if required

TYPICAL TIME CODE TRANSLATOR

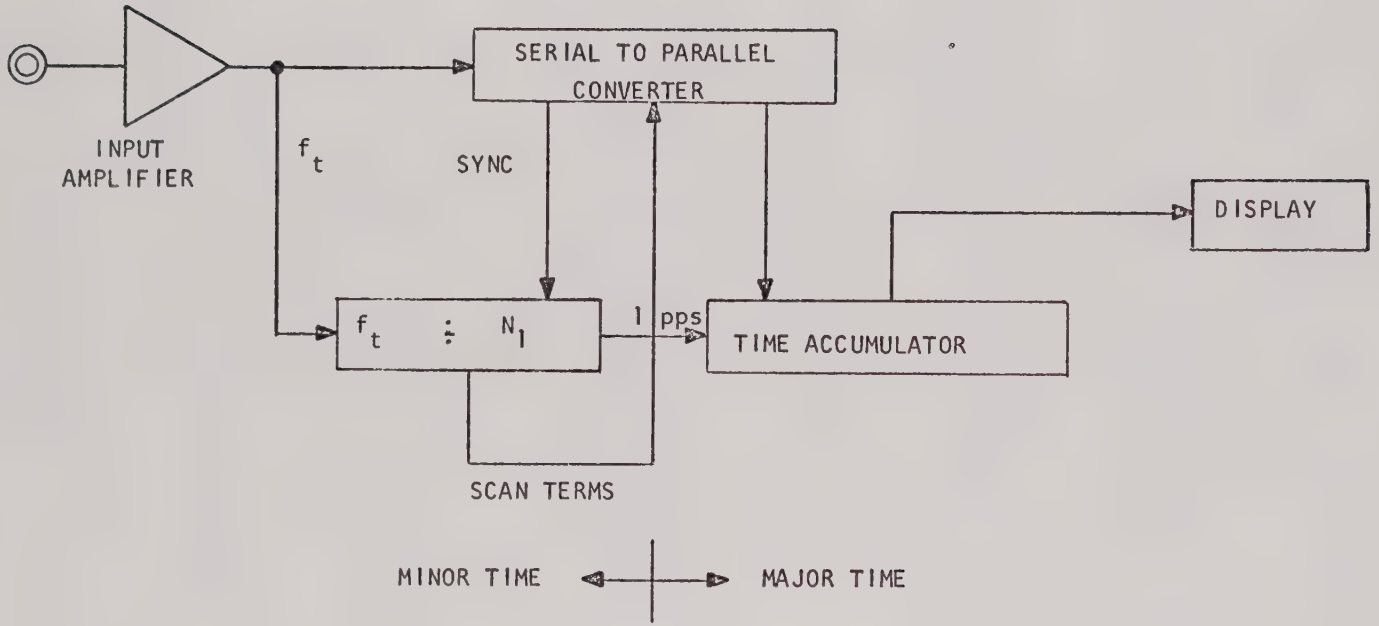


FIGURE 5-2

and it is contained in the input time code. The Time Accumulator is the basis for most outputs required by the unit.

e. Display - This section takes the Time Accumulator data and displays it for the user.

Now if we combine the two functions, taking advantage of circuitry found common to both, we obtain a Time Code Generator/Translator (Figure 5-3). Logic functions which are common, i.e., those which need not be duplicated are:

a. Frequency dividers (all of those in the translator and at least half of those in the generator).
b. Time Accumulator
c. Display

Of course, the power supply and chassis are shared.

5.3 DETAILED LOGIC DESCRIPTION

This description will be referenced only to the term reference numbers that are contained within the title block of each individual logic print. Before proceeding, the reader should be familiar with paragraph 5.1, LOGIC DESCRIPTION AND USE.

(1) AGC

The automatic gain control amplifier assembly contains the input amplifier and the code strippers required to normalize the input and derive the necessary clock signals for the decoder.

The AGC amplifier is wideband so as to make the unit operational where variations of input signal frequency as well as amplitude is experienced such as in tape search applications.

Generally if a translator is used as a single purpose unit such as to only translate code at a single rate and display it, the AGC circuits can be narrowband. To make the unit more adaptable to different types of applications, we have provided a 100 MV to 10 volt dynamic range and a frequency response of 25 Hz to 300 kHz. The circuit does not require adjustment over this range.

TYPICAL TIME CODE GENERATOR/TRANSLATOR

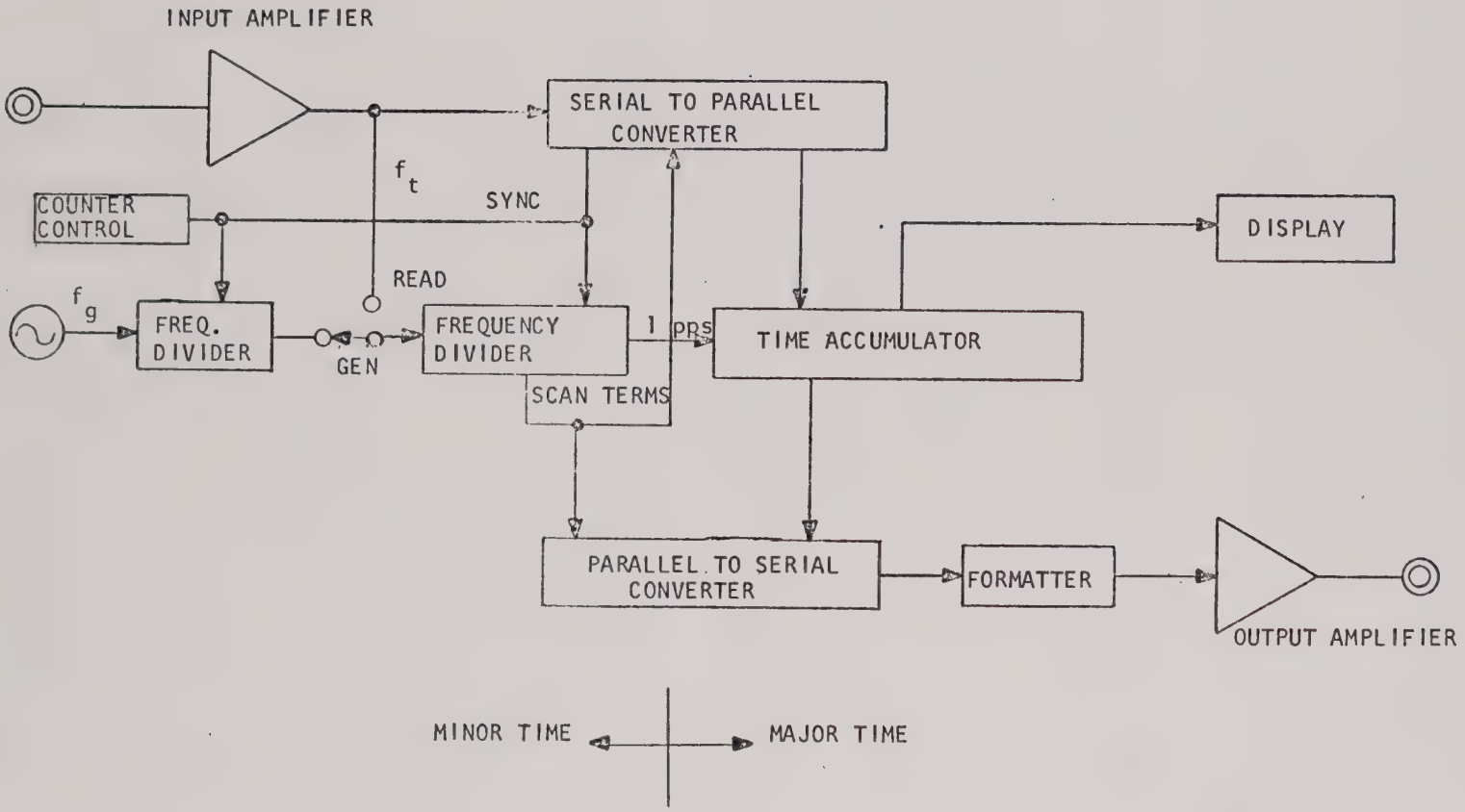


FIGURE 5-3

After the input signal is normalized by the AGC, preset level comparators develop clock signals used for decoding. ØA which occurs at the positive zero axis crossing of the carrier, is used throughout the unit for clocking and synchronization. ØC is the mark clock which occurs only each half cycle of the carrier modulation (mark amplitude cycles).

Figure 5-4 shows a typical modulated signal. Two cycles are modulated. Examples of ØA and ØC are shown relative to the signal. Observe also the other definitions provided.

(2)-(3) NASA Decoder - The output clocks from the AGC are connected to the decoder assembly; here the entire translation process takes place. The functions performed by the decoder assembly are:

a) Reconstruct dc envelope of the time code
b) Determine code pulse rate
c) Determine time frame sync (frame reference mark)
d) Synchronize minor time
e) Code bit storage and accumulator loading
f) Synchronization mode error detection and storage

Implementation of the decoder, which are of benefit to the user are described below:

a) DC Envelope Reformation - The amplitude modulation of the time code signal represents a pulse width modulated dc envelope. The key to reliable translation or reading is the reconstruction of the envelope. Once this has been done, it is a simple process to examine the dc signal for the presence of binary information. The clocks from the input shapers and three flip-flop storage counters are used in this operation. The significant point is that a cycle can be dropped or a noise spike can occur to add a pulse and the reconstruction of the envelope will not be affected. Thus, we say that the unit has "single cycle dropout protection".

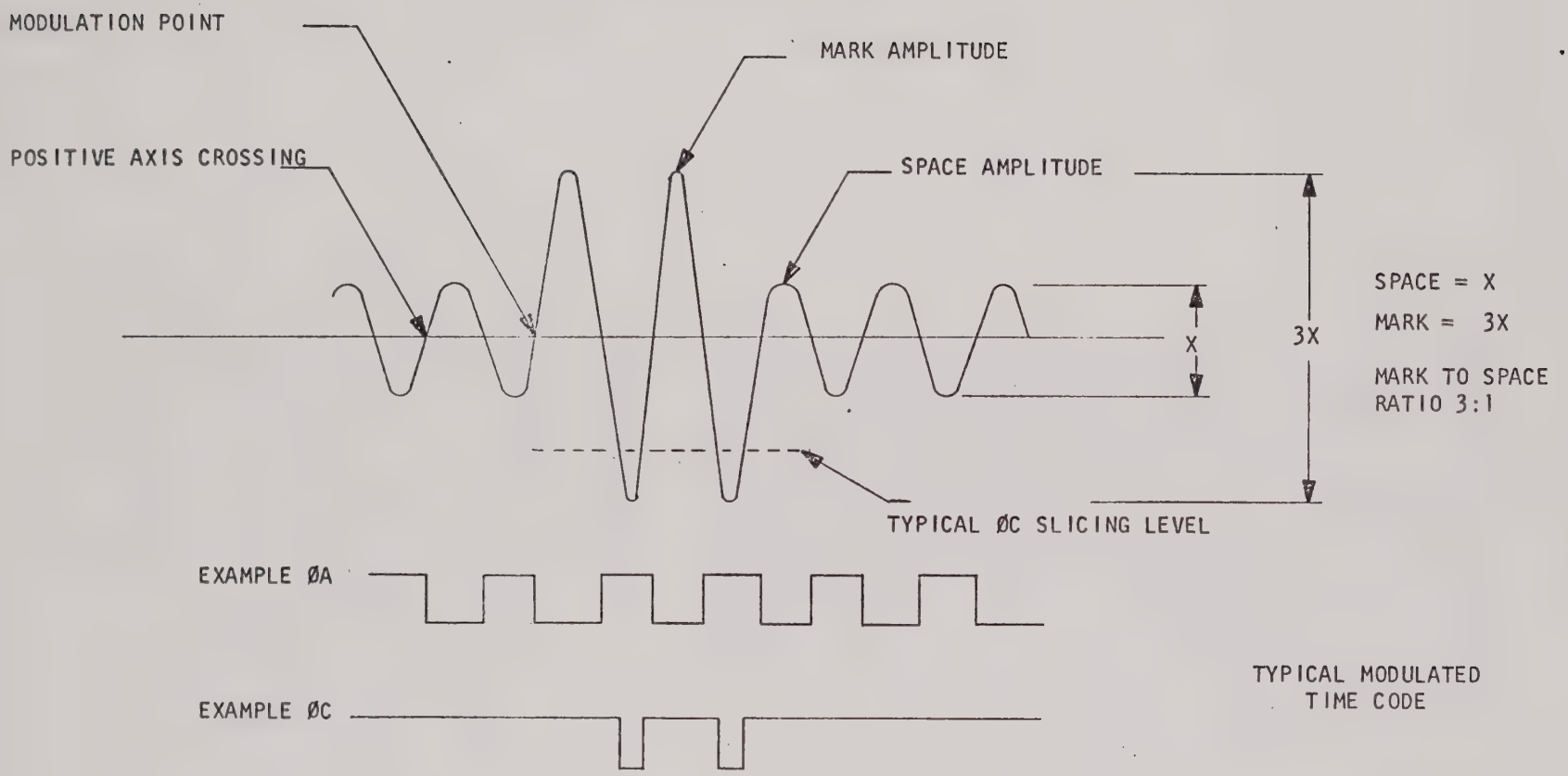

MODULATION POINT
MARK AMPLITUDE
POSITIVE AXIS CROSSING
SPACE AMPLITUDE
X
3X
SPACE = X
MARK = 3X
MARK TO SPACE RATIO 3:1
TYPICAL ØC SLICING LEVEL
EXAMPLE ØA
EXAMPLE ØC
TYPICAL MODULATED TIME CODE

FIGURE 5-4

b) Determine Code Pulse Rate - This is as simple as it appears. The first step to synchronization of the input is to detect the pulse rate of the input code. This is done by examining the dc envelope reconstructed in step (a) and developing a clock at the leading edge of this signal. In the NASA 36-bit format this clock would be 100 pps since the pulse rate of the coded information is 100 pps. This term is called "mark sync" (MS). For NASA 36-bit, the dc envelope obtained from the three counters in step (a) will be exactly 2 milliseconds late with respect to the "on time" point (modulation point) of the serial code. This is due to the logic implementation in the decoder discussed above. With MS occurring at 100 pps less 2 milliseconds, we know that the counter dividing 1 kHz must read "2" at its leading edge. Thus to synchronize the milliseconds counter all that is needed is to set it to a "2" with the MS clock. With the milliseconds counter synchronized, we now have a means to measure pulse widths of the input code from zero to 9 milliseconds.

c) Determine Frame Sync

d) Synchronize Minor Time

Let us summarize what we now know and have accomplished:

(1) We have a dc pulse train of the code.
(2) We have a counter dividing 1 kHz in synchronization with the dc code envelope. Thus, each code bit period is divided into 10 equal parts.
(3) The NASA 36-bit reference mark is five consecutive 6 millisecond bit periods.
(4) NASA 36-bit reference occurs at a 1 pps rate.

If we count and detect five consecutive 6 millisecond bit periods, we know we have received a 1 second reference. We also know that the counters counting 100 pps and 10 pps must be zero at this time. We therefore set them to zero of the leading edge of "F.S." (Frame Sync).

e) Code Bit Storage and Accumulator Loading - Now that we have a counter dividing 1 kHz (NASA 36-bit code carrier) and synchronized to the incoming code, we can locate any point within the format to a resolution of 1 millisecond. Furthermore, we can also "measure" the pulse width and therefore determine "1's" and "0's", which are noted to be of 6 and 2 millisecond duration, respectively.

A binary "1" is determined by examining the reconstructed dc envelope at a millisecond count of 6. A 4-bit shift register is successively loaded with the detected binary "1's" as they occur in the serial format. The result is therefore a continuous stream of "1's" and "0's" flowing through the 4-bit register.

Since the minor time counter (milliseconds, .01 seconds, .1 seconds) is synchronized with the input code, any 1 millisecond interval can be pin-pointed within the serial train. Actually, it is only necessary to locate an interval of 40 to 50 milliseconds -- in other words, an interval which contains 4 bits of code. Therefore, nine "load" periods are defined by gates "looking" at the minor time counter. Each of the load gates connects a 4-bit decade in the time accumulator to the shift register. As the data of interest is shifted in, it is loaded into the decade associated with the 4 bits. In this manner units of seconds, tens of seconds, units of

minutes, etc., are loaded sequentially from the shift register to the accumulator as the code is read.

The 36 bits of seconds, minutes, and hours and days are read and loaded in the first 900 milliseconds of the format. However, this time word represents a 1 second interval which began 900 milliseconds before (at the "on time" reference point). The output time must be placed "on time". That is, it is required that the output time update at the 1 second reference, which occurred 900 milliseconds before the entire time word is read. If, however, we take advantage of the fact that the synchronized minor time counter will supply a 1 pps signal exactly at the reference mark, we can then add this to the value in the accumulator. This, in effect, is anticipating the next time word value, and puts the output exactly "on time".

To summarize, the decoding process takes at least two time frame periods to synchronize to the code input. First, the code pulse rate synchronizes the least significant bit counter (milliseconds). Next, "frame sync" is determined by using this milliseconds data and the dc level envelope of the input code. This data allows complete synchronization of the minor time counter. Once this is done, "1's" and "0's" of the code can be located and placed in appropriate storage in the time accumulator. The accumulator is then updated with 1 pps to place it "on time". The entire process is repeated for each frame but does not actually cause any change in the output as long as the reader remains synchronized because the accumulator is being updated "on time" by the 1 pps pulse prior to the decoded time availability (900 milliseconds after "on time").

f. Synchronization Mode Error Detection and Storage - Another function contained on the decode assembly is the synchronization mode logic. In order to explain this function, it is necessary to assume that the unit is developing a serial code (before we have covered the serial code encoder section).

The "synchronization mode" function is designed to provide protection to the outputs in the event decoding errors occur. These errors can be due to many things such as noise, dropouts, voltage transients, etc. For example, if a noise burst or voltage transient occurred which caused a code error, thus wiping out a 1 second frame, the output would continue to read the correct code as long as carrier sync was maintained.

Obviously, if the carrier were gone completely for a time frame, the unit could not maintain sync. The synchronization mode feature increases the noise immunity of the unit significantly and is an added aid to tape search requirements.

The synchronization mode circuitry compares the reconstructed dc level with the generated code pulse train from the encoder. Thus, time contained in the time accumulator is compared bit-by-bit with the input code. If an error is detected, it is recorded and stored in the 3-bit counter. The next frame is examined. If another error is detected, it also is stored by adding it to the first, and so forth. Note that only one error per frame is considered.

The 9300 provides a front panel switch to select the error frame bypass mode. Six conditions are provided by the unit. These are:

(1) Zero Frames
(2) One Frame
(3) Two Frames
(4) Four Frames
(5) Eight Frames
(6) Infinite Frames

With "Two Frames" selected, the unit will accumulate two error frames without resynchronizing. If two consecutive errors are recorded, the next frame (third) is used to resynchronize the unit. The error counter is reset if no error is detected on the next frame (forth). If, however, an error condition continues, synchronization again is accomplished immediately. This is continued until two consecutive frames agree. Once synchronized, the unit "free runs:, so to speak, with synchronization disallowed until at least two consecutive frame errors are detected.

When "infinite" is selected, the synchronization of the unit is continuously inhibited and the unit acts as a generator using the carrier input as a clock.

With "Zero Frames" selected, the unit is a slave reader and synchronizes to each frame.

The number of frames desired to be bypassed is accomplished by selecting one of the six positions.

NASA DECODER (ENCODER) (6)

The NASA 36 Bit Time Code frame illustrated in Figure 1, consists of ten 100 millisecond sub-code word periods. Each word period is divided into ten 10 millisecond index periods. Thus, the status of the tenths-of-seconds counter can be used to identify sub-code word periods, while the status of the hundredths-of-seconds counter can be used to identify index periods within each sub-code word period.

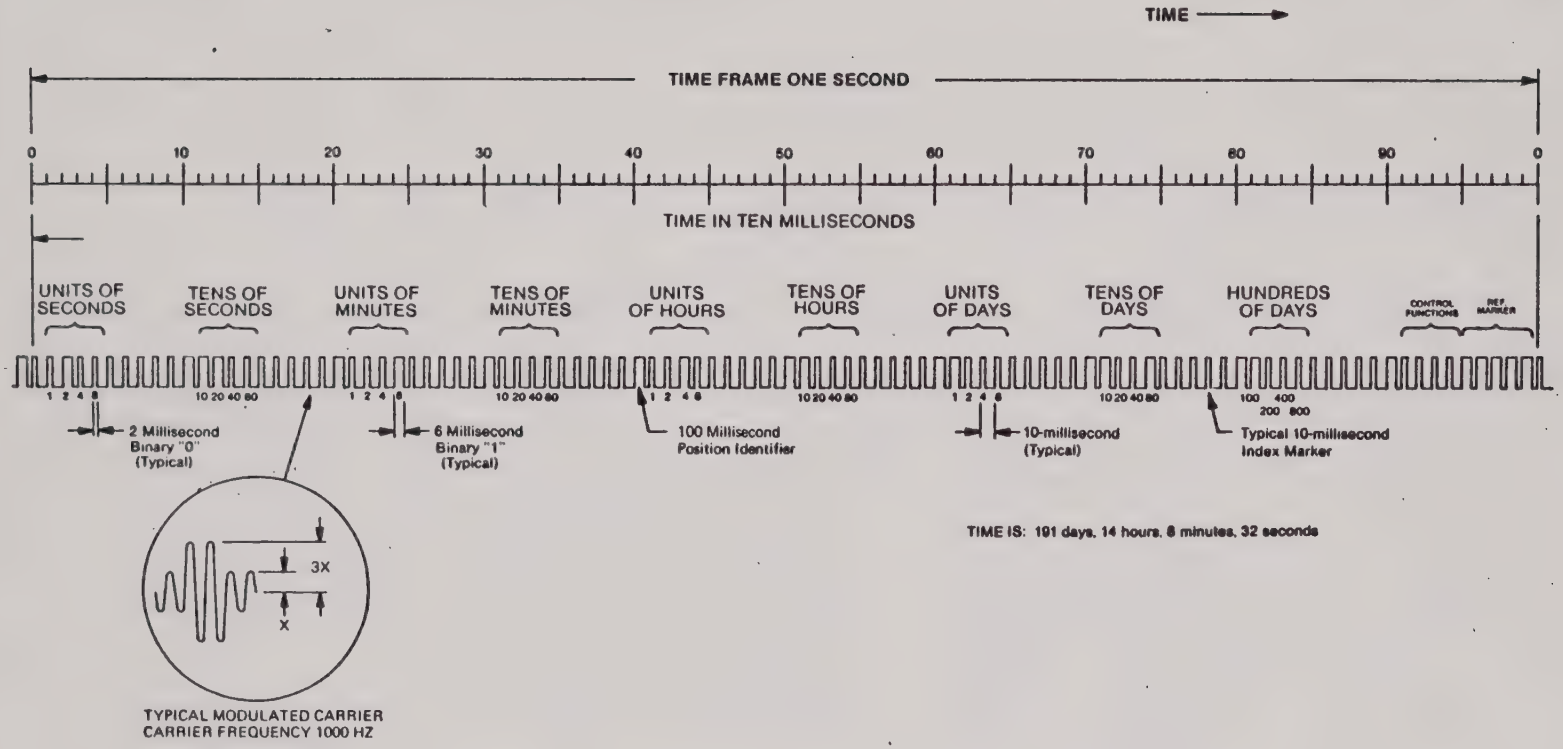
Logic Elements E2-5, are used to provide eight first rank multiplexers which scan the time data associated with the first eight subcode words of the time code frame. The multiplexers are enabled by a false hSC5 signal which is present only during the first five index periods of each sub-code word period. The outputs of these eight first rank multiplexers are obtained during each of the ten sub-code word periods of each time frame. However, second rank multiplexer element A15 is used to select each of these eight outpus during only one sub-code worder period.

Second rank multiplexer element E6 is enabled by a false level on the tSC8 line from the tenths-of-seconds counter (that is, it is enabled during the first eight sub-code word periods of each frame which are identified by the tenths-of-seconds counts of 0 through 7). The address inputs to the second rank multiplexer are tenths-of-seconds count signals tSC1, tSC2 and tSC4. These are connected so that the a, b, c, d, e, f, h, and j signals from the first rank multiplexer are connected to the second rank multiplexer output during tenths-of-seconds count periods 0, 1, 2, 3, 4, 5, 6, and 7 respectively.

The hundreds-of-days data associated with the ninth sub-code word and the control function data associated with the tenth sub-code word are scanned by the two multiplexers provided by the Logic Element E1. Each of these multiplexers is enabled only during the appropriate sub-code word period. Thus, no second rank multiplexing of the outputs of these two multiplexers is required.

Although the outputs of the K, L and N multiplexers are in a serial form. The data is not in the desired format. The NASA 36-Bit format is generated by flip-flop DCC. This flip-flop is clocked "true" at a 100 PPS rate at the beginning of each one-millisecond period. The reset time is determined by absence or presence of a binary one during each pulse period. If a binary "zero" is present (K, L and N outputs at zero), DCC reset enable occurs at plus one millisecond, and is clocked off on the next 1 KHz clock, producing a two-millisecond wide pulse. If a binary "one" is present, the reset enable is delayed until plus five milliseconds, producing a six-millisecond wide pulse.

During the last 50 milliseconds of each second, the output at A1 Pin 11 overrides the K, L and N multiplexers, producing a series of five binary one's, which is defined as the frame reference marker.



NASA 36-BIT TIME CODE (GENERAL)
(NASA 1 SECOND BCD TIME CODE)

1. **TIME FRAME:** 1 second
2. **CODE DIGIT WEIGHTING:** Binary Coded Decimal Time-of-Year CODE WORD — 30 binary digits. Seconds, minutes, hours and days; recycles yearly.
3. **CODE WORD STRUCTURE:** BCD: Word begins at INDEX COUNT 1. Binary-Coded Elements occur between POSITION IDENTIFIER ELEMENTS in 4-digit groups until the CODE WORD is complete. A CODE DIGIT occurs between decimal digits in each group to provide separation for visual resolution.
4. **LEAST SIGNIFICANT DIGIT:** Occurs first.
5. **ELEMENT RATES AVAILABLE:**
   a. 100 per second (basic Element Rate)
   b. 1 per second (Frame Rate)
6. **ELEMENT IDENTIFICATION:**
   a. "On-Time" reference point for each element is its leading edge.
   b. INDEX MARKER duration: 2 milliseconds (Binary zero or uncoded Element)
   c. CODE DIGIT duration: 6 milliseconds (Binary one)
   d. POSITION IDENTIFIER duration: 6 milliseconds
   e. REFERENCE MARKER: Five consecutive POSITION IDENTIFIERS followed by an INDEX MARKER.

   (The "On-Time" point, to which the CODE WORD refers, is the leading edge of the INDEX MARKER following the four POSITION IDENTIFIERS.)
7. **RESOLUTION:** 10 milliseconds (unmodulated); 1 millisecond (modulated).
8. **CARRIER FREQUENCY:** 1 kHz when modulated.

FIGURE 1

NASA 36-BIT ONE-SECOND TIME CODE

NASA DECODER (OSC LOGIC) (7)

This logic illustrates the four standard time base options available for the 9300. Refer to the top assembly drawing for the time base installed in this instrument.

NASA DECODER (MINOR TIME) (8)

This logic consists of a series of decimal counter units (DCU) which take the 1 MHz clock from (7) and divides it by one million to provide six decades of BCD clock terms, microseconds through tenths of seconds.

Also contained are buffers for the four standard pulse rates and a one-shot for providing the sample time strobe pulse for the parallel outputs.

NASA DECODER (MAJOR TIME) (9)

This logic consists of a series of divide-by-ten and divide-by-six DCU's which which permute this 1 PPS clock (cUSC) from (8) into nine decades of BCD time-of-year. The hours counters are reset to zero at the end of 23 hours by one-shot RHC.

In the read mode, the Major Time counter is preset to the decoded contents of the input code (SF1, 2, 4, 8) by nine strobe terms, $\overline{\text{SUSC}}$ through $\overline{\text{SHDC}}$ from the decoder (3). In the generate mode, these counters are preset to the contents of the thumbwheel switch on the front panel via the load terms $\overline{\text{SUSC}}$* through $\overline{\text{SHDC}}$*.

NASA DECODER (DISPLAY DRIVERS) (10)

This logic consists of nine four-to-seven-line decoders and current limiting resistor packs. The BCD outputs of the major time counter (9) are converted to the seven-line format required to drive the front panel display.

INTERFACE (11)

This drawing interfaces the front and rear panels with the logic boards contained within this instrument.

LED DISPLAY (12)

This logic consists of nine seven-segment light-emitting diode display units which convert the seven-line outputs from (10) into a visual time display, representing generated or decode time-of-year in seconds, minutes, hours and days.

POWER SUPPLY (49)

The Power Supply furnishes regulated ±15V DC and +5V DC to the unit. The ±15V DC regulators are integrated circuit regulators with internal fault protection. The +5V DC regulator employs and LM305 voltage regulator and is of the switching type.

The LM305 is essentially an operational amplifier with a built-in Zener reference. When the voltage on pin 6 falls a few millivolts below that of the internal reference, Q1 and Q2 are turned off and the voltage on A1-6 rises above the reference level. L1 tries to maintain constant current flow and current begins to flow through CR2. This continues until Q1 and Q2 are again turned on and the cycle is repeated.

The switching regulator is thus an efficient method of obtaining constant 5V DC from an unregulated source, since power is dissipated in Q1 only when it is on or changing states.

For 5 volts from a 23V source, Q1 is on approximately 25 percent of the time. Q3 and Q4 provide short circuit protection by forcing the regulator to decrease the output voltage when the current through R7 becomes excessive. When the output voltage becomes too high, CR5 conducts and CR6 is turned on. The current limit circuit then shuts down the regulator.

OPTIONS

Described in the following paragraphs are some (but not all) of the options and capabilities which are available. For instance, Control Functions and/or Binary seconds can be encoded and inserted into the serial code formats or translated from the input codes. These particular capabilities, although not listed would most likely be used in conjunction with one or more of the other options.

ADVANCE/RETARD (20) (OPTION)

When in the generator mode of operation this assembly, in conjunction with front panel switches, allows the operator to slew the internally generated update clock in order to align it with an external reference signal.

EXTERNAL START (25) (OPTION)

Allows the unit to be started "on time" from an external WWV TICK signal or a DC pulse.

17 BIT BINARY CONVERTER (27) (OPTION)

Provides parallel buffered 17 bit Binary outputs (seconds, minutes, hours) of the major time counter. 10 bits of Binary milliseconds can also be provided.

SLOW CODE (29) (OPTION)

Converts parallel BCD information (Major Time), in conjunction with a front panel switch, to a bi-level 5 rate serial Slow Code format.

PARALLEL OUTPUTS (30) (OPTION)

Provides parallel buffered BCD outputs of the major and or minor time counter contents. Also provides for other output timing signals and for external control of the Time Code Translator (e.g. Tape Search Control) if required.

SECTION VI
MAINTENANCE

The 9300 Time Code Generator/Translator utilizes integrated circuits. There are no moving parts or parts with limited life. There is no periodic maintenance required for the unit under normal conditions. If the unit is exposed to unusual operating conditions such as high dust or high humidity environments, or if the unit is dropped or otherwise damaged, it may be necessary to perform certain inspections and/or repairs.

If it is necessary to inspect the unit, the following should be considered:

1. Always disconnect AC power before removing the instrument cover. To remove the cover, simply remove the screw at the rear panel and slide the cover off to the rear.

2. Make a thorough visual inspection of all circuitry and wiring.

3. Check for physical integrity of all components. Look for burned or cracked components, loose physical damage, leakage of insulation compounds or general physical damage. To aid in overall maintenance and repair, each integrated circuit is mounted in an individual modular socket. Removal or replacement is therfore convenient and easy.

   It should rarely be necessary to replace an integrated circuit; however, if replacement is attempted, be sure that all component leads enter the socket and that no leads are bent under the component or extended out from the socket.

   Check to see that all IC's are firmly mounted in the socket so that good electrical contact is made.

4. Check all switches and connectors for loose or broken wires.

5. If the internal component surfaces and components have an excessive amount of dust deposited on them, use a soft brush and a low pressure stream of air to remove any foreign material.

CAUTION

Do not clean PC boards or small internal components with a stiff brush or solvents since damage to the circuits may result. A high powered vacuum cleaner device should not be used on small internal components.

6. Wipe the external surfaces of the instrument with a soft damp cloth to remove dirt, fingerprints and other foreign material.

7. Replace the cover and reconnect the AC power and input connector. Check operation. If performance does not match or exceed the specifications listed, corrective maintenance is in order.

Printed Circuit Board Repair

Removal and insertion of IC components can be easily made as described above. Should it be necessary to replace conventional components which are soldered to the circuit board, cut the leads of the part near the lead holes. Using a low power (50 watts or less) soldering iron, apply heat sparingly to each cut lead. As soon as the solder melts, slip the lead from the hole and clean the hole with a tooth pick. Clean the board surfaces with isopropyl alcohol. Form the tinned leads of the replacement part and insert in cleaned holes, trimming the leads to extend 1/16-inch beyond the back surface of the board. Only 63/37 solder with a maximum

diameter of 1/16 inch should be used. Solder the leads to the board and use a hemostat, long nosed pliers, or other heat sink on the leads of all semiconductor devices and quarter-watt resistors. Allow the soldered junction to cool before removing the heat sink.

WARNING

Dangerous high voltages are present in the unit. Use caution at all times when the protective cover is removed.

SECTION VII

LIST OF DRAWINGS

1.	Top Assembly	9300-7323
2.	AGC (1)	16085 A-16085
3.	NASA Decoder (2) (3) (6) (7) (8) (9) (10)	16446
4.	Switch & Control Logic (11)	9300-8715
5.	LED Display (12)	16447
6.	Shaper Modulator (15) (15A)	17056 A-17056
7.	Power Supply (49)	16280 A-16280
8.	S/H Register (51) (52)	16989 A-16989
9.	I/O Control (50) (50A) (50B)	18180 A-18180

REVISIONS			
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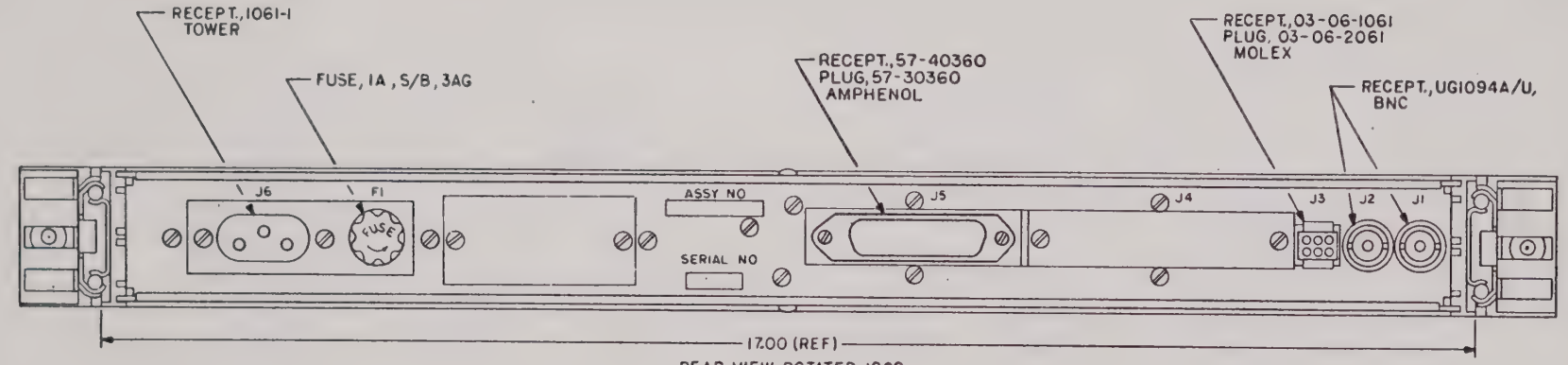
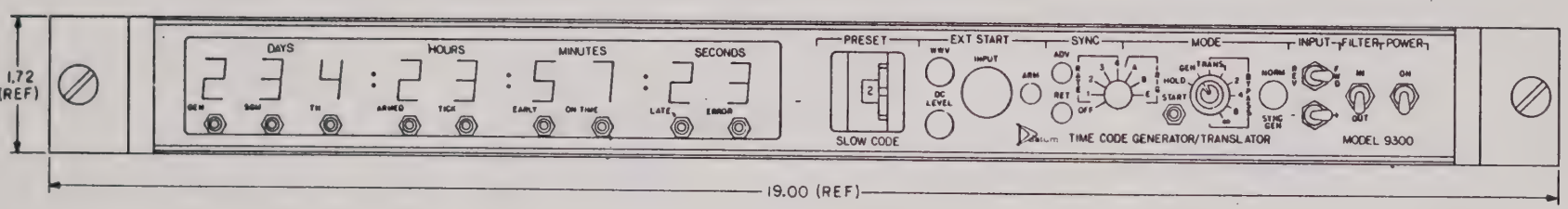


REAR VIEW ROTATED 180°



5. SWITCH & CONTROL LOGIC 9300-8715
4. WIRING DIAGRAM 804040
3. WIRE LIST 809349 (UNIT)

J6-AC POWER
J5-I/O CONTROL
J4-
J3-PULSE RATE OUTPUTS
J2-CODE OUTPUT } NASA 36
2. J1-CODE INPUT }
1. SLIDES & MOUNTING BRACKETS ARE OPTIONAL

NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1°

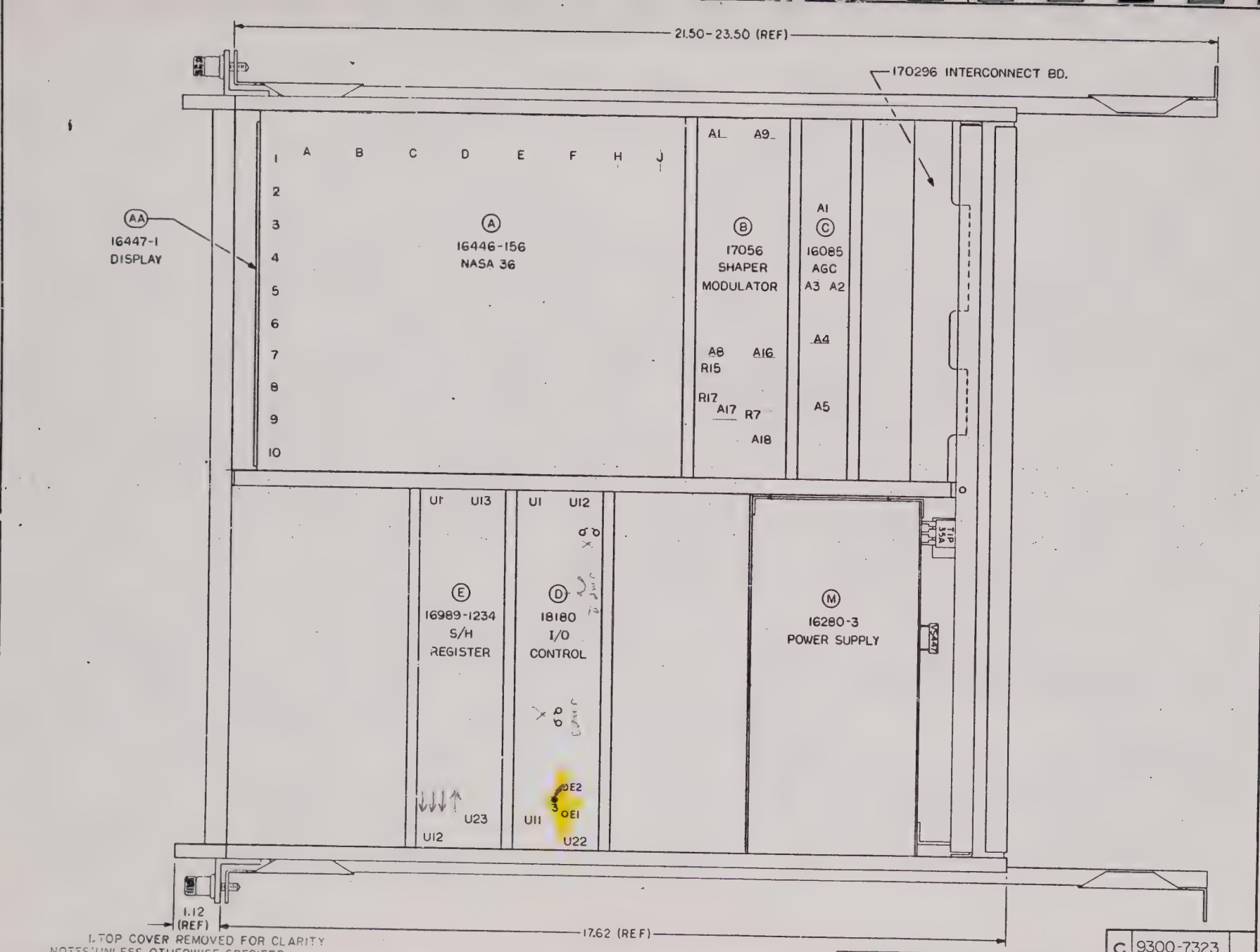
TITLE: TIME CODE GENERATOR/TRANSLATOR

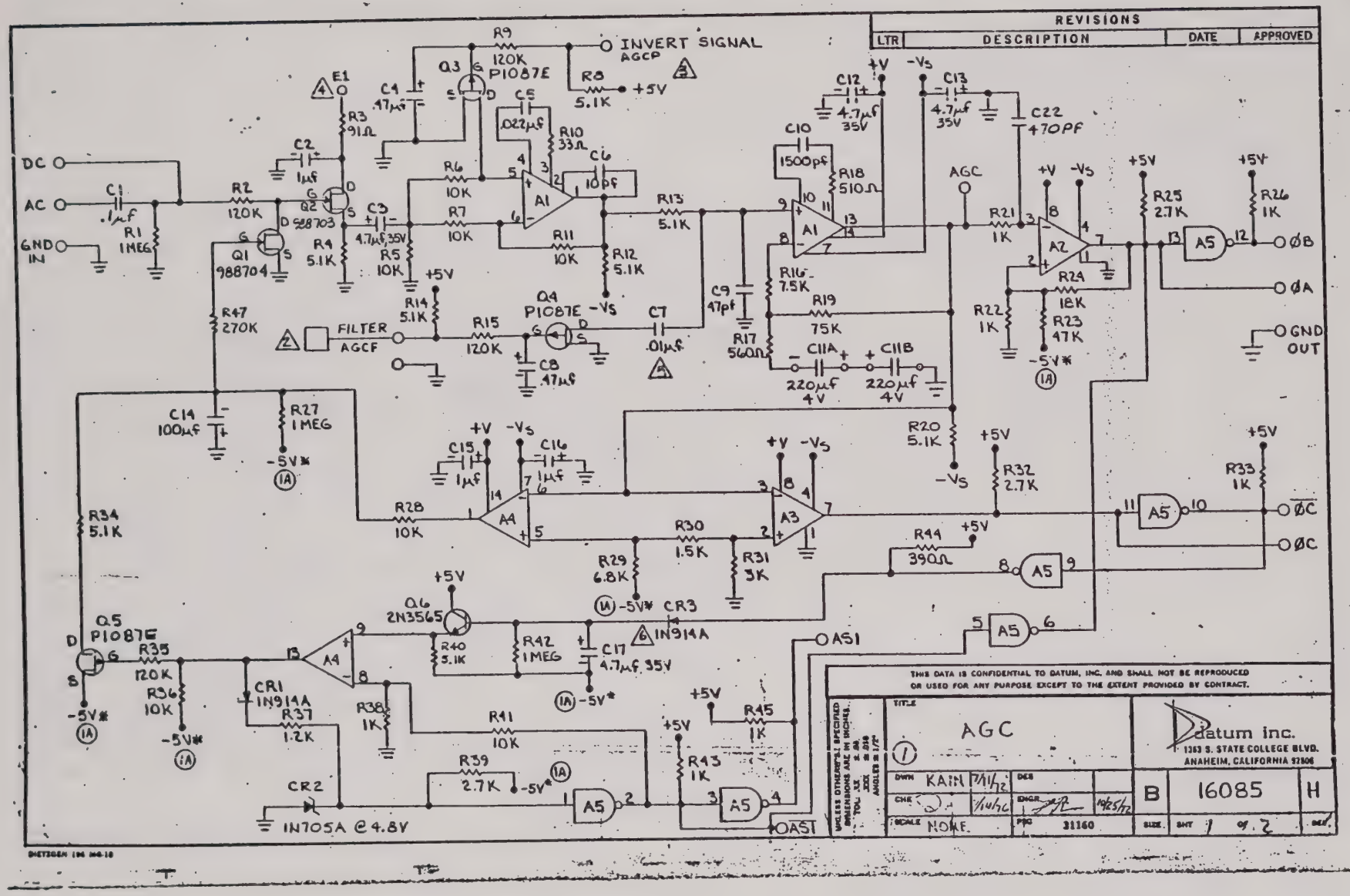
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

DWN	LUCAS	2-24-84	DES		
CHK	CFE	2-24-84	ENGR	HAMMOND	3/15/84
SCALE	NONE		FSC	31160	

C 9300-7323

SIZE | SHT 1 OF 2 | REV


21.50-23.50 (REF)
170296 INTERCONNECT BD.
AA
16447-1
DISPLAY
A
16446-156
NASA 36
B
17056
SHAPER
MODULATOR
C
16085
AGC
A3 A2
A4
A5
A1
A9
A8
A16
R15
R17
A17
R7
A18
E
16989-1234
S/H
REGISTER
D
18180
I/O
CONTROL
M
16280-3
POWER SUPPLY
U13
U12
U23
U11
U22
OE2
OE1
TIP
35A
1.12
(REF)
17.62 (REF)
1. TOP COVER REMOVED FOR CLARITY
NOTES: UNLESS OTHERWISE SPECIFED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
C
9300-7323
SIZE
SHT 2 OF 2
REV


REVISIONS
LTR
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DATE
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AGCP
FILTER
AGCF
AGC
DC
AC
GND IN
GND OUT
ØA
ØB
ØC
ØC
AS1
OAST
+5V
-Vs
-5V*
Q1 988704
Q2 988703
Q3 P1087E
Q4 P1087E
Q5 P1087E
Q6 2N3565
A1
A2
A3
A4
A5
R1 1MEG
R2 120K
R3 91Ω
R4 5.1K
R5 10K
R6 10K
R7 10K
R8 5.1K
R9 120K
R10 33Ω
R11 10K
R12 5.1K
R13 5.1K
R14 5.1K
R15 120K
R16 7.5K
R17 560Ω
R18 510Ω
R19 75K
R20 5.1K
R21 1K
R22 1K
R23 47K
R24 18K
R25 2.7K
R26 1K
R27 1MEG
R28 10K
R29 6.8K
R30 1.5K
R31 3K
R32 2.7K
R33 1K
R34 5.1K
R35 120K
R36 10K
R37 1.2K
R38 1K
R39 2.7K
R40 5.1K
R41 10K
R42 1MEG
R43 1K
R44 390Ω
R45 1K
R47 270K
C1 .1μf
C2 1μf
C3 4.7μf,35V
C4 .47μf
C5 .022μf
C6 10pf
C7 .01μf
C8 .47μf
C9 47pf
C10 1500pf
C11A 220μf 4V
C11B 220μf 4V
C12 4.7μf 35V
C13 4.7μf 35V
C14 100μf
C15 1μf
C16 1μf
C17 4.7μf,35V
C22 470PF
CR1 IN914A
CR2 IN705A @4.8V
CR3 IN914A
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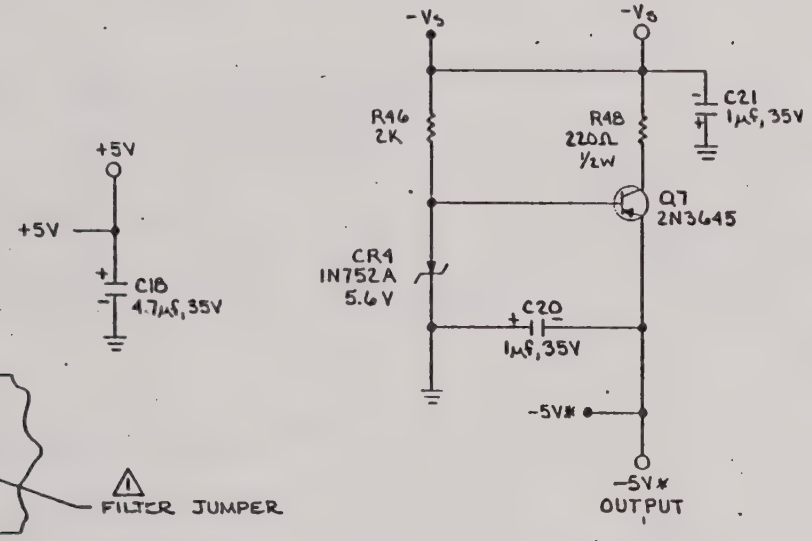
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°
TITLE
AGC
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806
DWN KAIN 7/11/72
CHK 7/14/72
ENGR 10/25/72
SCALE NONE
PRO 31160
SIZE B
16085
H
SHT 1 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ADDED C22	9-27-72	R.F.
B	ADDED R20 TO SCHEMATIC +E WAS +Vs	1-22-73	[illegible]
C	Q3,4,5 WERE 2N4342	6-13-73	R.F.
D	ADDED C11A & C11B	7-13-73	[illegible]
E	Q1 WAS 988703	9-12-73	R.F./C.V
F	C12 & C13 WERE 1 µf	9-21-73	[illegible]/C.V
G	R3 WAS TO +E, ADDED E1	11-26-73	[illegible]/R.S.
H	ADDED 6	7-7-79	C.A.



6 -2 C17 IS 27µf 10V, R27 IS 4.7M

5 -1 C7 IS .001µf.

4 WIRE TO +15 OR +5V AS REQUIRED

3 THIS POINT GROUNDED TO INVERT SIGNAL - REVERSE MODE

2 SEE PARALLEL OUTPUT SCHEM FOR PIN NUMBER

1 REMOVE FOR REMOTE OR HIGHSPEED OPERATION

PART NO	MFR	REF
SN7405	NATIONAL	A5
µA749	FAIRCHILD	A1, A4
LM311H	NATIONAL	A2, A3

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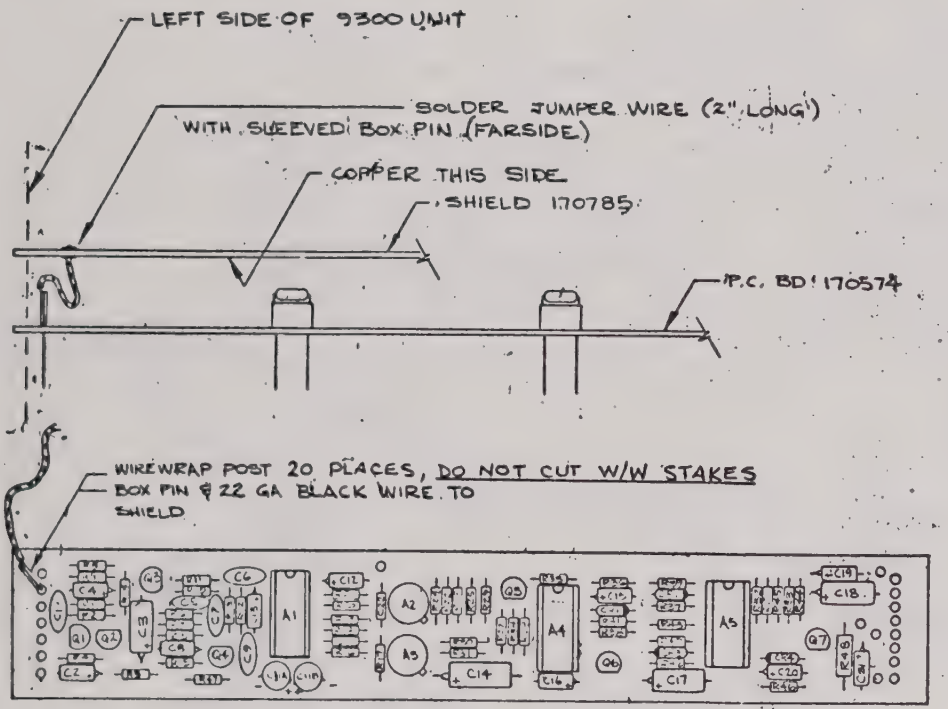
TITLE: AGC (1A)

DWN KAIN 7/12/72 | DES RF 7/12/72 | CHK [illegible] 7/19/72 | ENGR [illegible] 7/25/72 | SCALE NONE | FSC 31160

datum inc. 1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92806

B | 16085 | H | SIZE | SHT 2 OF 2 | REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
—	REMOVED EYET FROM SHIELD	1-4-79	STEVE


LEFT SIDE OF 9300 UNIT
SOLDER JUMPER WIRE (2" LONG)
WITH SLEEVED BOX PIN (FARSIDE)
COPPER THIS SIDE
SHIELD 170785
P.C. BD 170574
WIREWRAP POST 20 PLACES, DO NOT CUT W/W STAKES
BOX PIN & 22 GA BLACK WIRE TO
SHIELD

REF A/N NO 170574

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .02 .XXX ± .010 ANGLES ± 1/2°

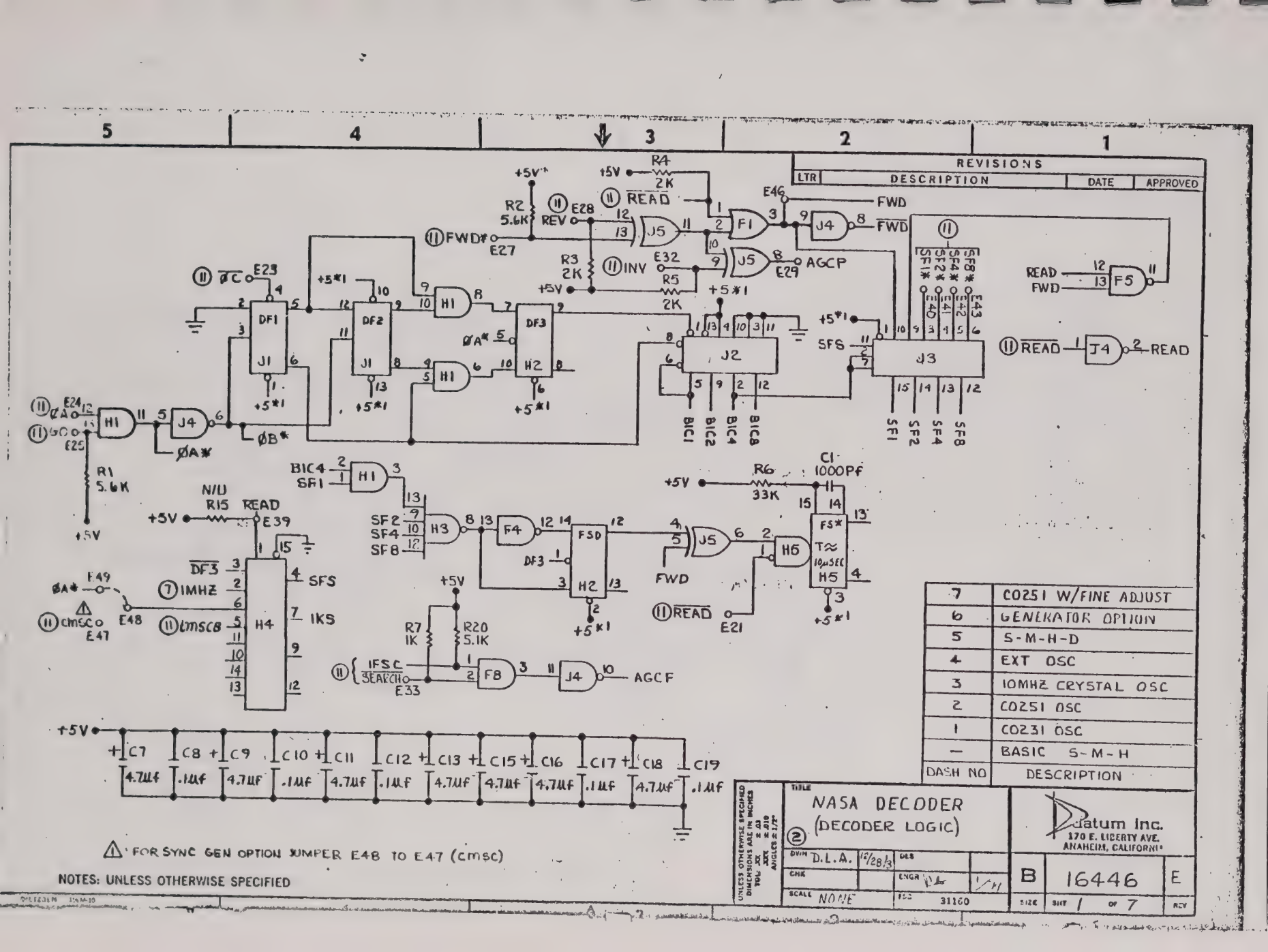
TITLE: ASSEMBLY AID AGC

datum inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA

DWN	MILES	5/1/73	DES	KF	5/1/73
CHK			ENGR		
SCALE	1:1		FSC	31160	

B | A-16085 | H

SIZE | SHT 1 OF 1 | REV



DASH NO	DESCRIPTION
7	CO251 W/FINE ADJUST
6	GENERATOR OPTION
5	S-M-H-D
4	EXT OSC
3	10MHZ CRYSTAL OSC
2	CO251 OSC
1	CO231 OSC
—	BASIC S-M-H

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03 .XXX ± .010 ANGLES ± 1/2°

TITLE: NASA DECODER (DECODER LOGIC) ②

Datum Inc. 170 E. LIBERTY AVE. ANAHEIM, CALIFORNIA

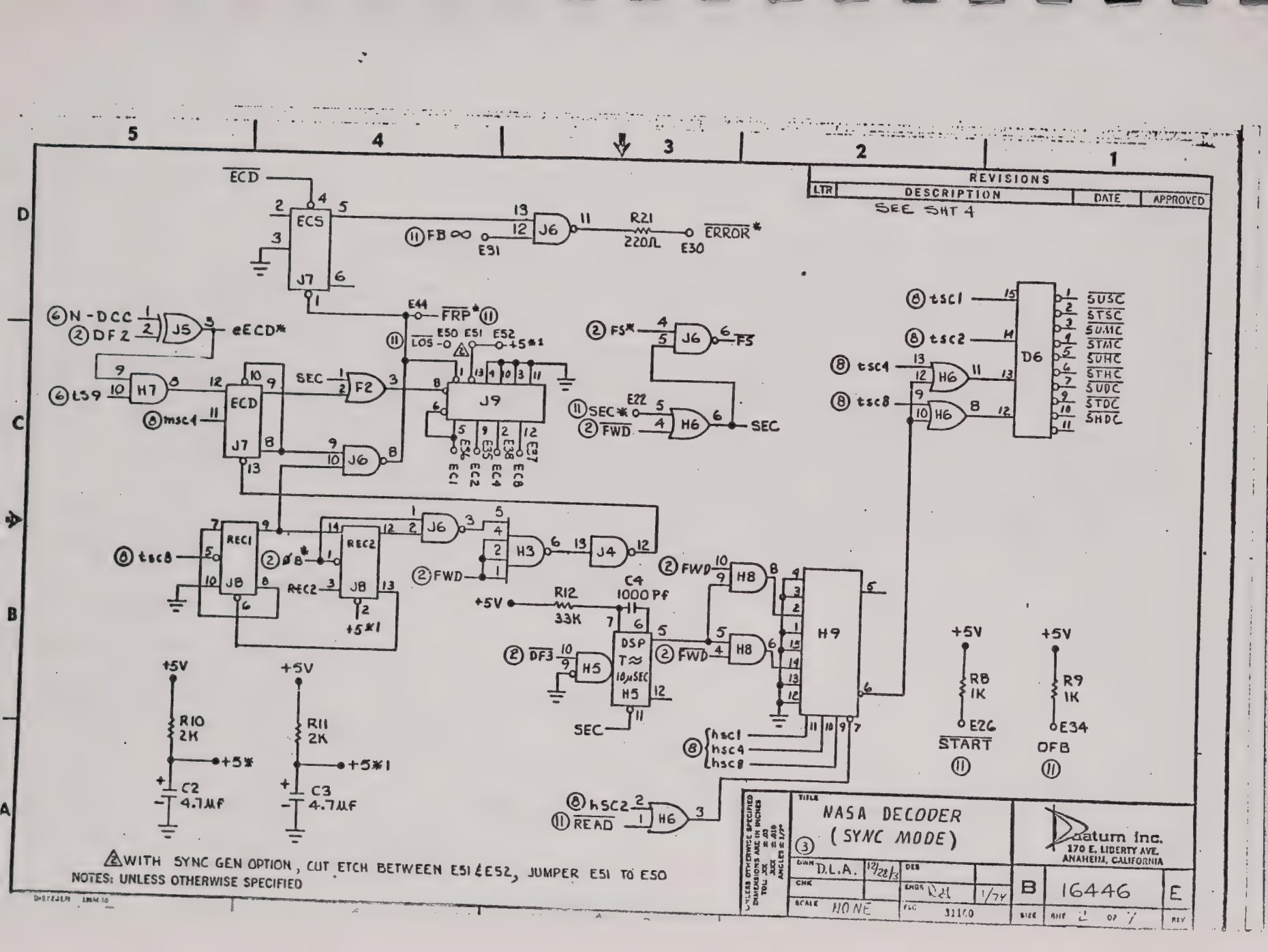
DWN D.L.A. 12/28/73 DES

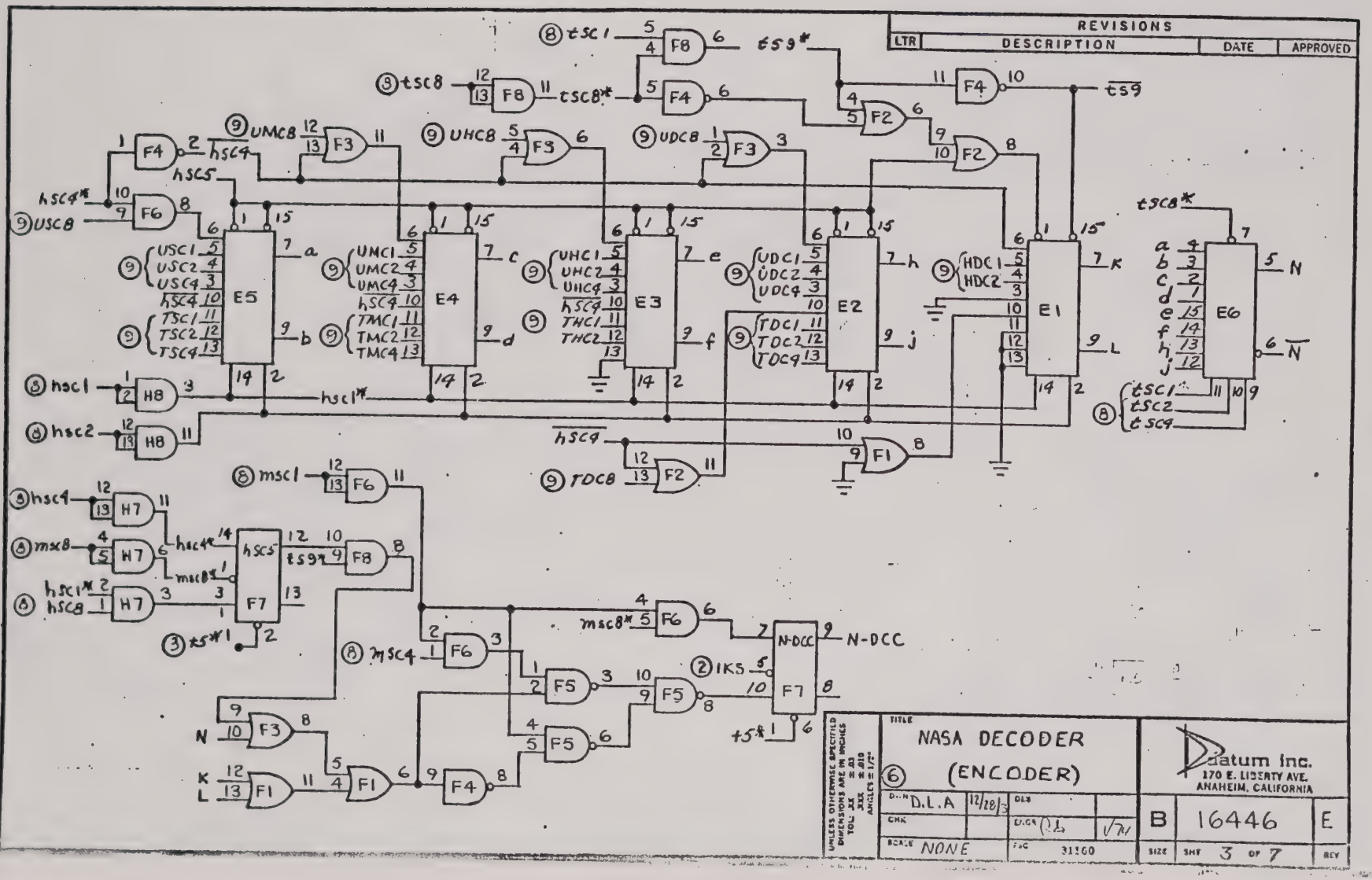
CHK ENGR 1/74

SCALE NONE FSC 31160

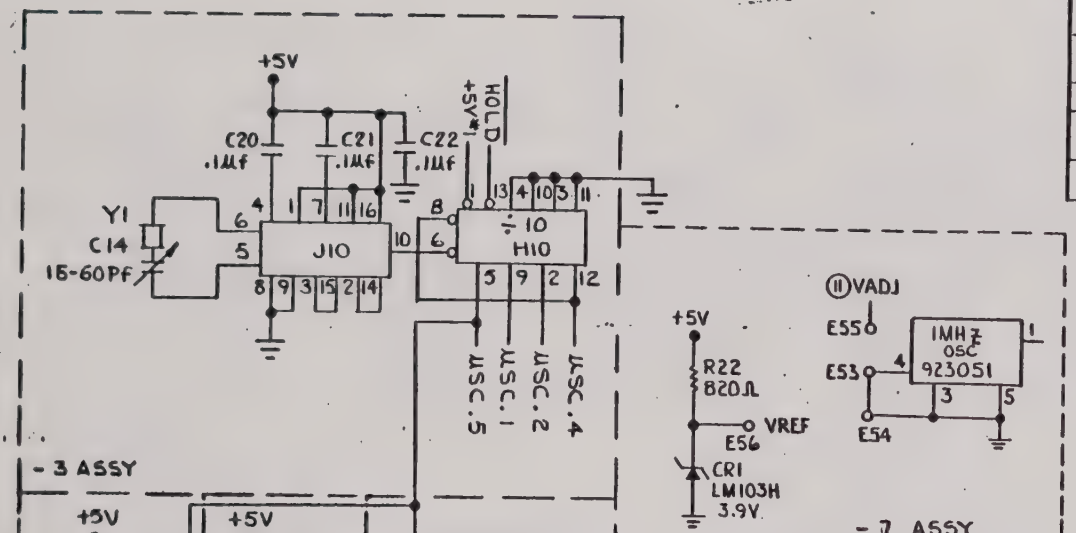
B 16446 E

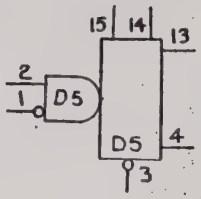
SIZE SHT 1 OF 7 REV


REVISIONS
LTR DESCRIPTION DATE APPROVED
SEE SHT 4
ECD
ECS
J7
J6
R21
220Ω
ERROR*
E30
E31
FB∞
E44
FRP*
N-DCC
DF2
J5
eECD*
LOS-0
ES0 ES1 ES2
+5*1
H7
LS9
ECD
J7
msc1
SEC
F2
J9
J6
EC1 EC2 EC4 EC8
F5*
F5
SEC*
E22
FWD
H6
SEC
tsc1
tsc2
tsc4
tsc8
D6
SUSC
STSC
SUMC
STMC
SUHC
STHC
SUDC
STDC
SHDC
REC1
REC2
J8
J6
H3
J4
FWD
+5*1
R12
33K
C4
1000 Pf
DSP
T≈
10μSEC
H5
DF3
SEC
H8
H9
hsc1
hsc4
hsc8
+5V
RB
1K
E26
START
R9
1K
E34
OFB
R10
2K
+5*
C2
4.7MF
R11
2K
+5*1
C3
4.7MF
hsc2
READ
H6
WITH SYNC GEN OPTION, CUT ETCH BETWEEN ES1 & ES2, JUMPER ES1 TO ES0
NOTES: UNLESS OTHERWISE SPECIFIED
TITLE
NASA DECODER
(SYNC MODE)
③
DWN D.L.A. 12/28/73
CHK
SCALE NONE
DES
ENGR 1/74
APP 3110
Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
B 16446 E
SIZE SHT 2 OF 7 REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
NASA DECODER
(ENCODER)
Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
D.L.A
12/28/83
NONE
31160
B
16446
E
SHT 3 OF 7
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL .XX ±.03
.XXX ±.010
ANGLES ±1/2°
F1
F2
F3
F4
F5
F6
F7
F8
H7
H8
E1
E2
E3
E4
E5
E6
N-DCC
hsc1
hsc2
hsc4
hsc5
hsc9
msc1
msc4
msc8
tsc1
tsc2
tsc8
tsc9
tsc9*
hsc1*
hsc4*
hsc8*
msc8*
tsc8*
N-DCC
USC1
USC2
USC4
TSC1
TSC2
TSC4
UMC1
UMC2
UMC4
TMC1
TMC2
TMC4
UHC1
UHC2
UHC4
THC1
THC2
UDC1
UDC2
UDC4
TDC1
TDC2
TDC4
HDC1
HDC2
IKS
+5*1
N
K
L

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	R3 WAS TO GND, J4-3&4 WERE NOT USED PER CO# 2181	5-12-75	RM
B	ADDED R20,21, J4-10&11 WERE NOT USED PER C.O. 3533	12-17-76	IC
C	ADDED NOTES PERTAINING TO SYNC GEN OPTION	11-22-77	S.V.
D	ADDED E47-56 R21 & CR1 PER CO.4068	2-21-78	IC
E	REVISE PER C.O. T3722	2-12-79	L.S.





NOT USED

NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .010 XXX ± .005 ANGLES ± 1/2°

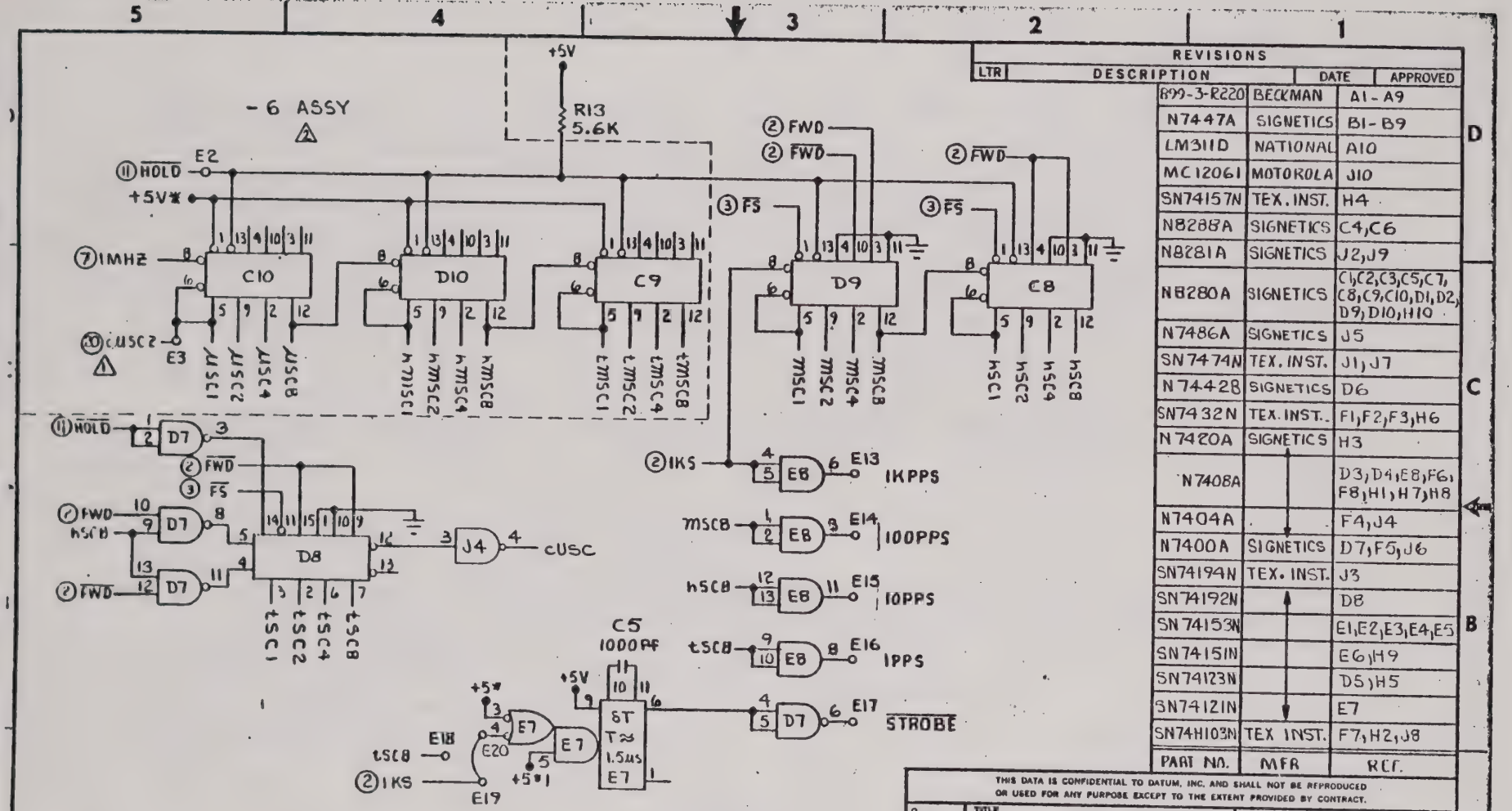
TITLE: NASA DECODER (TIME BASE) ⑦

DWN	D.L.A 12/31/	DES	
CHK		ENGR	1/14
SCALE	NONE	FSC	31160

datum inc. 1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92806

SIZE			REV
B	16446	SHT 4 OF 7	E

DIETZGEN



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

PART NO.	MFR	REF.
899-3-R220	BECKMAN	A1 - A9
N7447A	SIGNETICS	B1 - B9
LM311D	NATIONAL	A10
MC12061	MOTOROLA	J10
SN74157N	TEX. INST.	H4
N8288A	SIGNETICS	C4, C6
N8281A	SIGNETICS	J2, J9
N8280A	SIGNETICS	C1, C2, C3, C5, C7, C8, C9, C10, D1, D2, D9, D10, H10
N7486A	SIGNETICS	J5
SN7474N	TEX. INST.	J1, J7
N74428	SIGNETICS	D6
SN7432N	TEX. INST.	F1, F2, F3, H6
N7420A	SIGNETICS	H3
N7408A		D3, D4, E8, F6, F8, H1, H7, H8
N7404A		F4, J4
N7400A	SIGNETICS	D7, F5, J6
SN74194N	TEX. INST.	J3
SN74192N		D8
SN74153N		E1, E2, E3, E4, E5
SN7415IN		E6, H9
SN74123N		D5, H5
SN7412IN		E7
SN74H103N	TEX INST.	F7, H2, J8

(4) WHEN SYNC GEN OPTION IS INSTALLED ALL -6 TERMS ORIGINATE ON (15)
(1) TERM USED WITH ADVANCE/RETARD OPTION; ETCH CUT BETWEEN C10-5,6
NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ±.010 .XXX ±.005 ANGLES ±1/2°

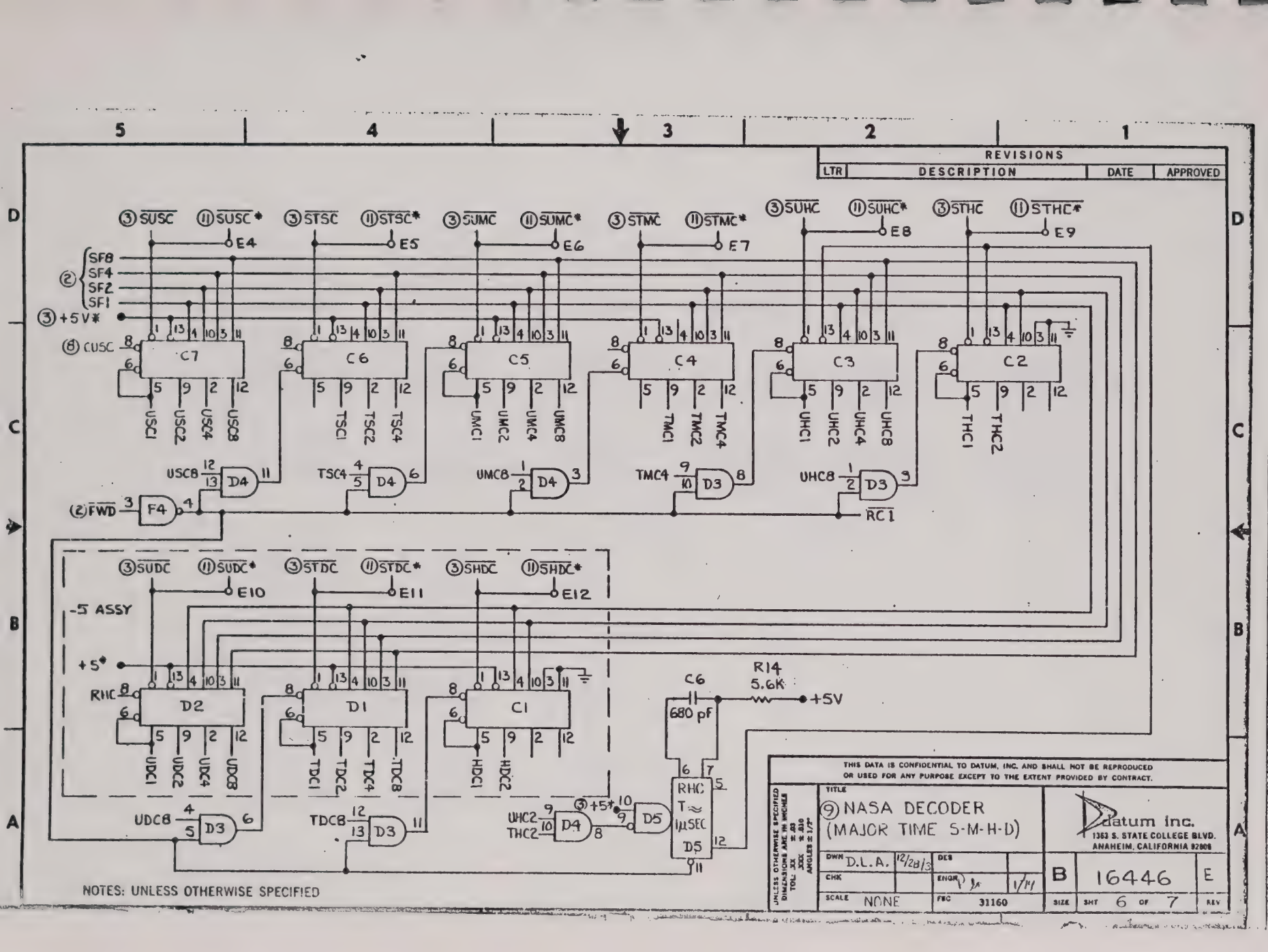
TITLE: NASA DECODER (8) (MINOR TIME)

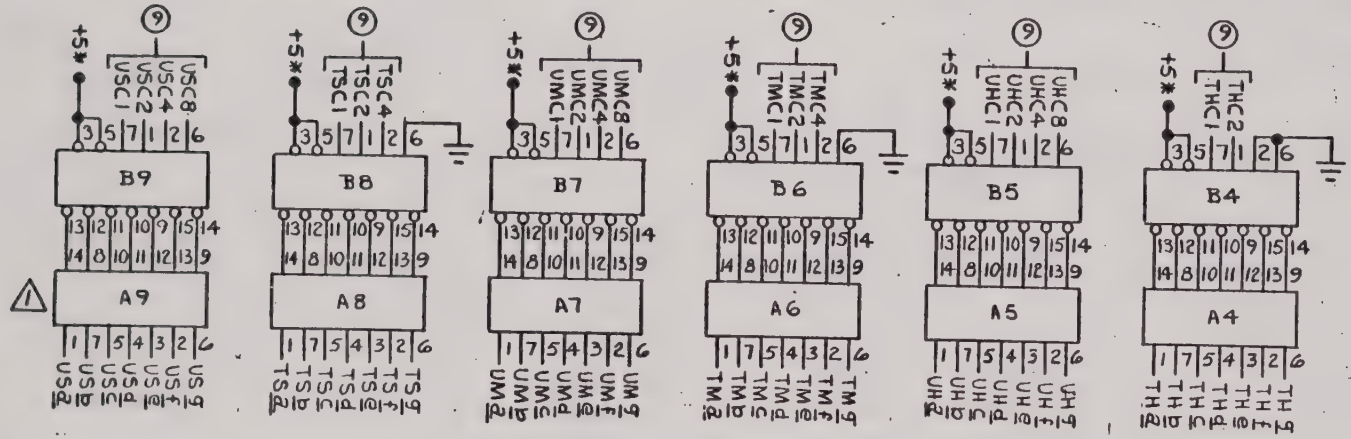
DWN D.L.A 12/28/73 | DES | CHK | ENGR RG 1/74 | SCALE NONE | FSC 31160

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B | 16446 | E

SIZE | SHT 5 OF 7 | REV


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
③ SUSC
⑪ SUSC*
③ STSC
⑪ STSC*
③ SUMC
⑪ SUMC*
③ STMC
⑪ STMC*
③ SUHC
⑪ SUHC*
③ STHC
⑪ STHC*
E4
E5
E6
E7
E8
E9
② SF8
SF4
SF2
SF1
③ +5V*
⑧ CUSC
C7
C6
C5
C4
C3
C2
USC1
USC2
USC4
USC8
TSC1
TSC2
TSC4
UMC1
UMC2
UMC4
UMC8
TMC1
TMC2
TMC4
UHC1
UHC2
UHC4
UHC8
THC1
THC2
USC8
TSC4
UMC8
TMC4
UHC8
D4
D4
D4
D3
D3
② FWD
F4
RC1
③ SUDC
⑪ SUDC*
③ STDC
⑪ STDC*
③ SHDC
⑪ SHDC*
E10
E11
E12
-5 ASSY
+5*
RHC
D2
D1
C1
UDC1
UDC2
UDC4
UDC8
TDC1
TDC2
TDC4
TDC8
HDC1
HDC2
C6
680 pF
R14
5.6K
+5V
RHC
T≈ 1μSEC
D5
UDC8
TDC8
UHC2
THC2
D3
D3
D4
D5
③ +5*
NOTES: UNLESS OTHERWISE SPECIFIED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03 XXX ± .010 ANGLES ± 1/2°
TITLE
⑨ NASA DECODER (MAJOR TIME S-M-H-D)
DWN D.L.A. 12/28/73
CHK
ENGR 1/14
SCALE NONE
DES
FSC 31160
datum inc.
1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92806
B
16446
E
SIZE
SHT 6 OF 7
REV



1 A1-A9 ARE 220Ω, 1/4 W RESISTOR PACKS

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED

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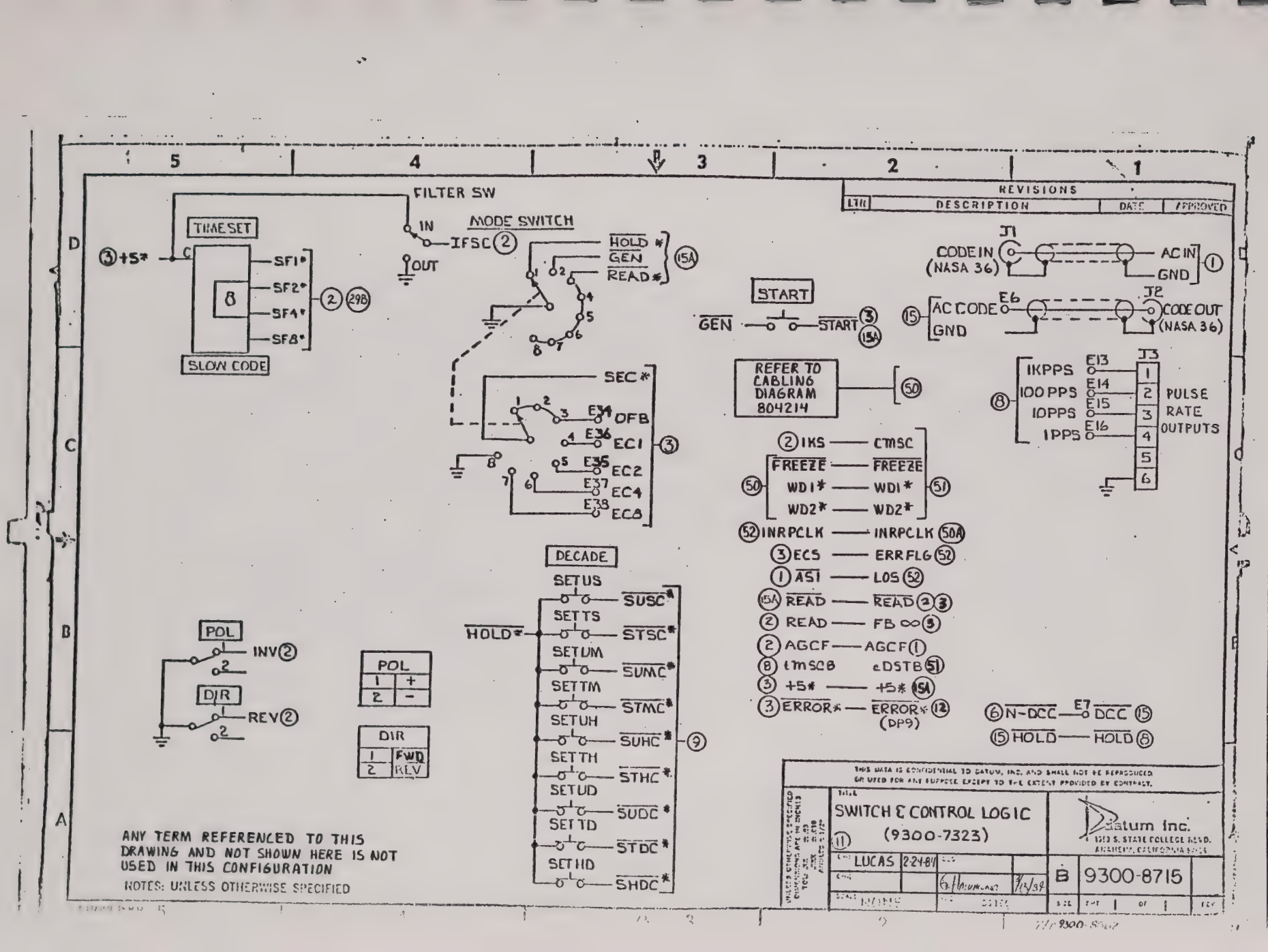
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL .XX ± .03, .XXX ± .010, ANGLES ± 1/2°

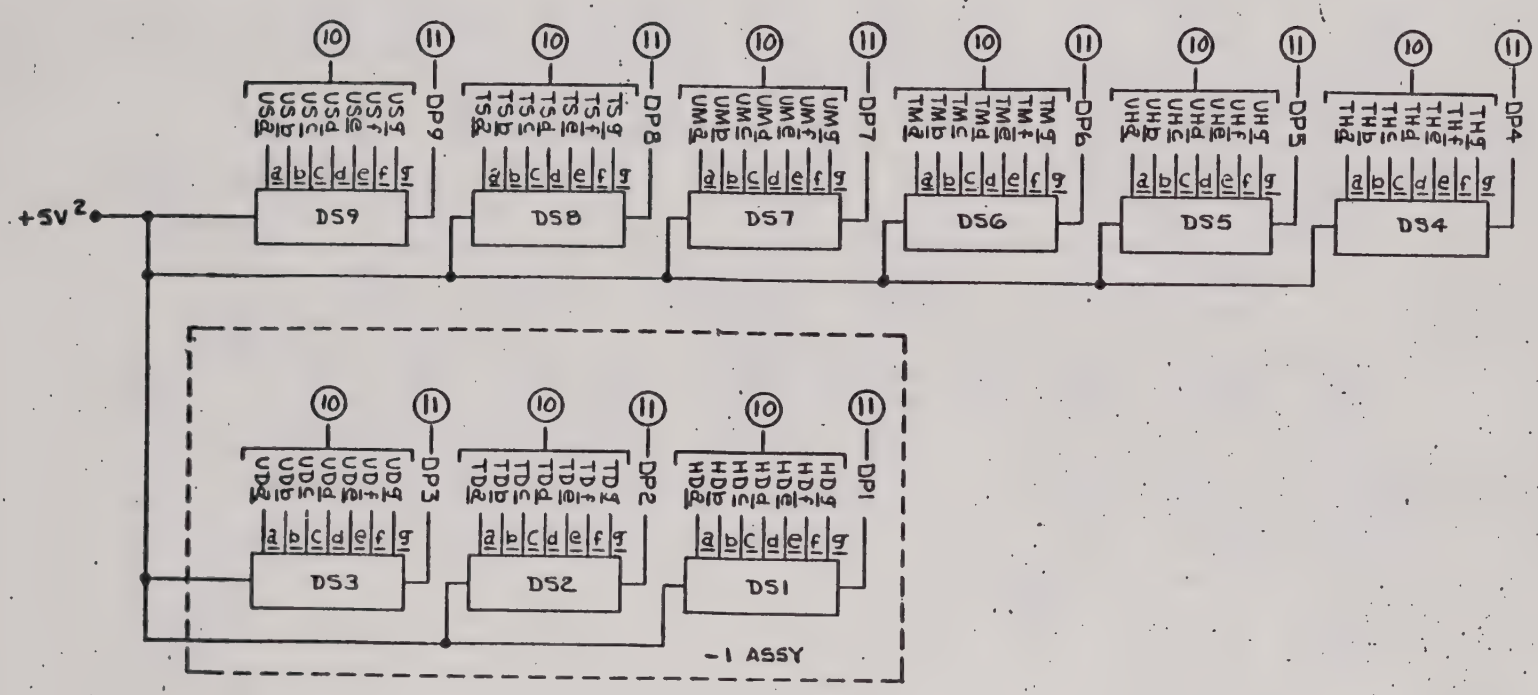
TITLE: NASA DECODER (10) (DISPLAY DRIVERS)

datum inc. 1363 S. STATE COLLEGE BLVD. ANAHEIM, CALIFORNIA 92806

DWN	D.L.A	12/20/73	DES			
CHK			ENGR	D.G	1/74	
SCALE	NONE		FSC	31160	SIZE B	16446 E
					SHT 7 OF 7	REV


FILTER SW
IN
OUT
IFSC (2)
MODE SWITCH
HOLD *
GEN
READ *
(15A)
TIME SET
(3) +5*
C
B
SF1*
SF2*
SF4*
SF8*
(2) (29B)
SLOW CODE
SEC*
OFB
EC1
EC2
EC4
EC8
(3)
START
GEN
START (3)
(15A)
REFER TO CABLING DIAGRAM 804214
(50)
J1
CODE IN (NASA 36)
AC IN
GND
(1)
J2
(15) AC CODE
GND
E6
CODE OUT (NASA 36)
J3
(8)
1KPPS E13
100 PPS E14
10PPS E15
1PPS E16
PULSE RATE OUTPUTS
(2) IKS — CMSC
FREEZE — FREEZE (50) (51)
WD1* — WD1*
WD2* — WD2*
(52) INRPCLK — INRPCLK (50A)
(3) ECS — ERRFLG (52)
(1) ASI — LOS (52)
(15A) READ — READ (2) (3)
(2) READ — FB ∞ (5)
(2) AGCF — AGCF (1)
(8) CMSCB — CDSTB (51)
(3) +5* — +5* (15A)
(3) ERROR* — ERROR* (12) (DP9)
(6) N-DCC — E7 DCC (15)
(15) HOLD — HOLD (8)
POL
INV (2)
DIR
REV (2)
POL
1 +
2 -
DIR
1 FWD
2 REV
DECADE
HOLD*
SETUS — SUSC*
SETTS — STSC*
SETUM — SUMC*
SETTM — STMC*
SETUH — SUHC* (9)
SETTH — STHC*
SETUD — SUDC*
SETTD — STDC*
SETHD — SHDC*
ANY TERM REFERENCED TO THIS DRAWING AND NOT SHOWN HERE IS NOT USED IN THIS CONFIGURATION
NOTES: UNLESS OTHERWISE SPECIFIED
REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.
TITLE
SWITCH & CONTROL LOGIC (9300-7323)
(11)
Datum Inc.
LUCAS 2-24-84
B
9300-8715
SCALE NONE
SHEET 1 OF 1
9300-8502

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	HP 5082-7650 WERE HP 5082-7750	6-11-77	



-3 DS1-9 ARE FAIRCHILD FND-507
-2 DS1-9 ARE MONSANTO MAN6A
1. DS1-9 ARE H/P 5082-7650
NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03 XXX ± .010 ANGLES ± 1/2°

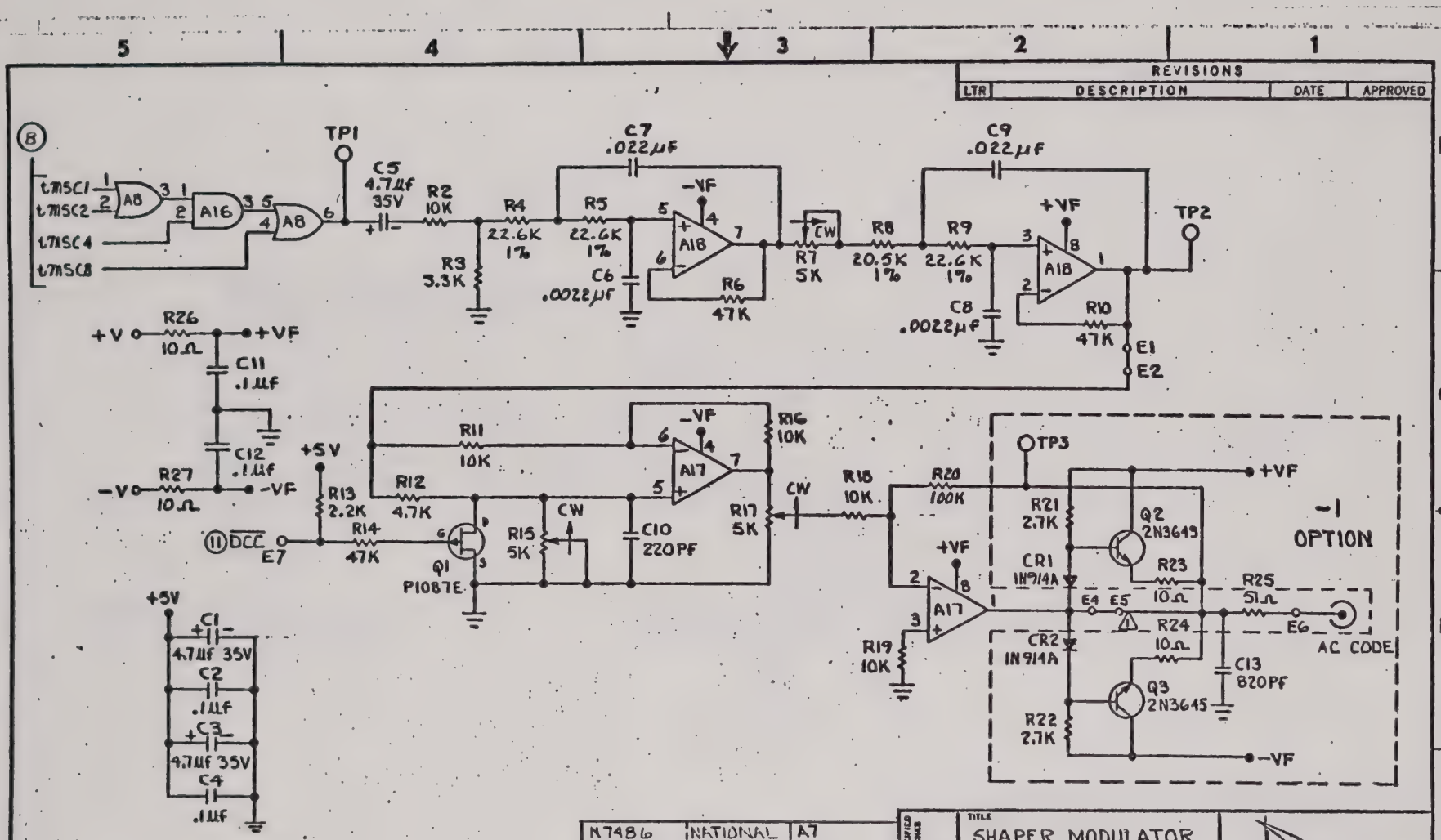
TITLE: LED DISPLAY (12)

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

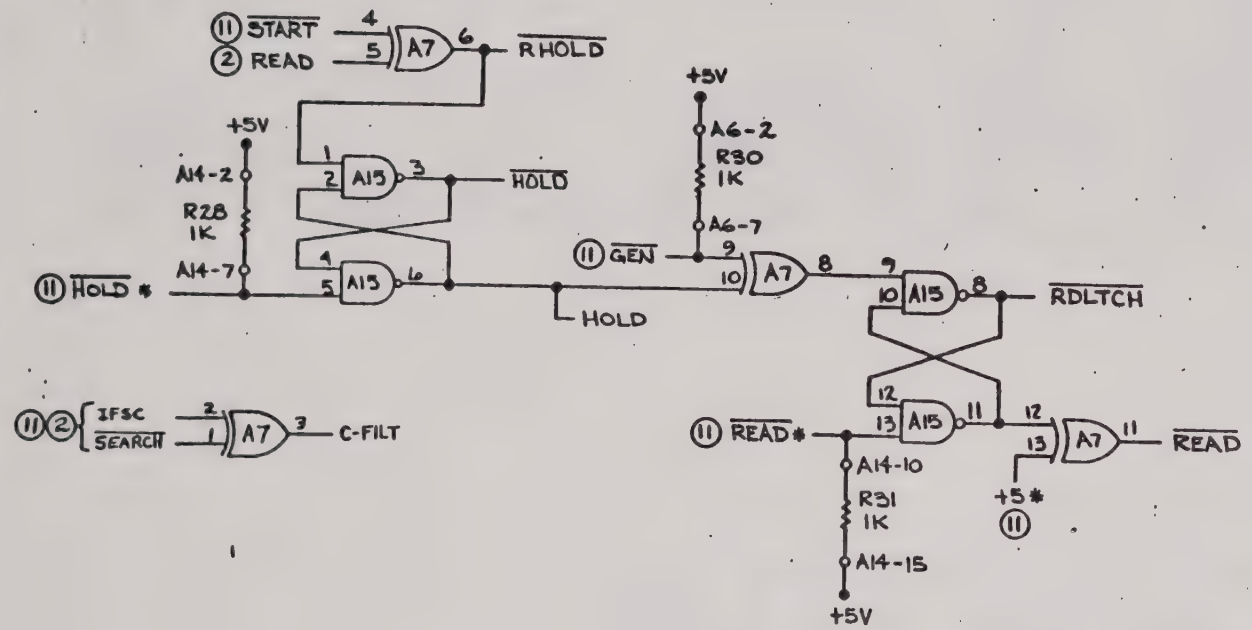
DWN	D.L.A.	1/3/74	DES		
CHK			ENGR		1/74
SCALE	NONE		FSC	31160	

B | 16447 | A

SIZE | SHT | OF | REV


REVISIONS
LTR DESCRIPTION DATE APPROVED
TP1
C5 4.7µf 35V
R2 10K
R4 22.6K 1%
R5 22.6K 1%
C7 .022µF
-VF
A18
R6 47K
C6 .0022µF
R3 3.3K
R7 5K CW
R8 20.5K 1%
R9 22.6K 1%
C9 .022µF
+VF
TP2
C8 .0022µF
R10 47K
E1
E2
tMSC1
tMSC2
tMSC4
tMSC8
A8
A16
R26 10Ω
+V
+VF
C11 .1µF
C12 .1µF
R27 10Ω
-V
-VF
+5V
R11 10K
R12 4.7K
R13 2.2K
R14 47K
R15 5K CW
C10 220PF
R16 10K
R17 5K
A17
Q1 P1087E
DCC E7
R18 10K CW
R20 100K
TP3
R21 2.7K
Q2 2N3643
CR1 IN914A
R23 10Ω
R25 51Ω
E4 E5 E6
AC CODE
-1 OPTION
R24 10Ω
CR2 IN914A
C13 820PF
Q3 2N3645
R22 2.7K
R19 10K
C1 4.7µf 35V
C2 .1µF
C3 4.7µf 35V
C4 .1µF
⚠ CUT ETCH IF -1 OPTION INSTALLED
NOTES: UNLESS OTHERWISE SPECIFIED
N7486 NATIONAL A7
N7400A NATIONAL A15
N5558V SIGNETICS A17, 18
N7432 NATIONAL A8
N7406 NATIONAL A16
PART NO. MFR REF
TITLE
SHAPER MODULATOR
15
Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA
DWN VALENCIA
DES
ENGR
SCALE NONE
B 17056
SHT 1 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ±.02 .XXX ±.010 ANGLES ± 1/2°

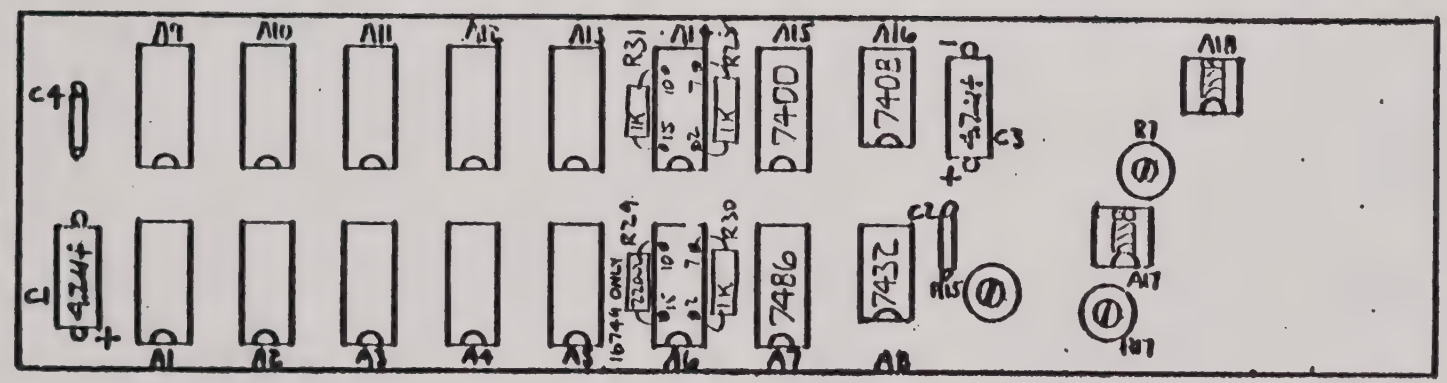
TITLE: SHAPER MODULATOR

15A

DWN VALENCIA 12-23-76 | DES | CHK | ENGR | SCALE | FSC 31160

Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B | 17056 | SIZE | SHT 2 OF 2 | REV



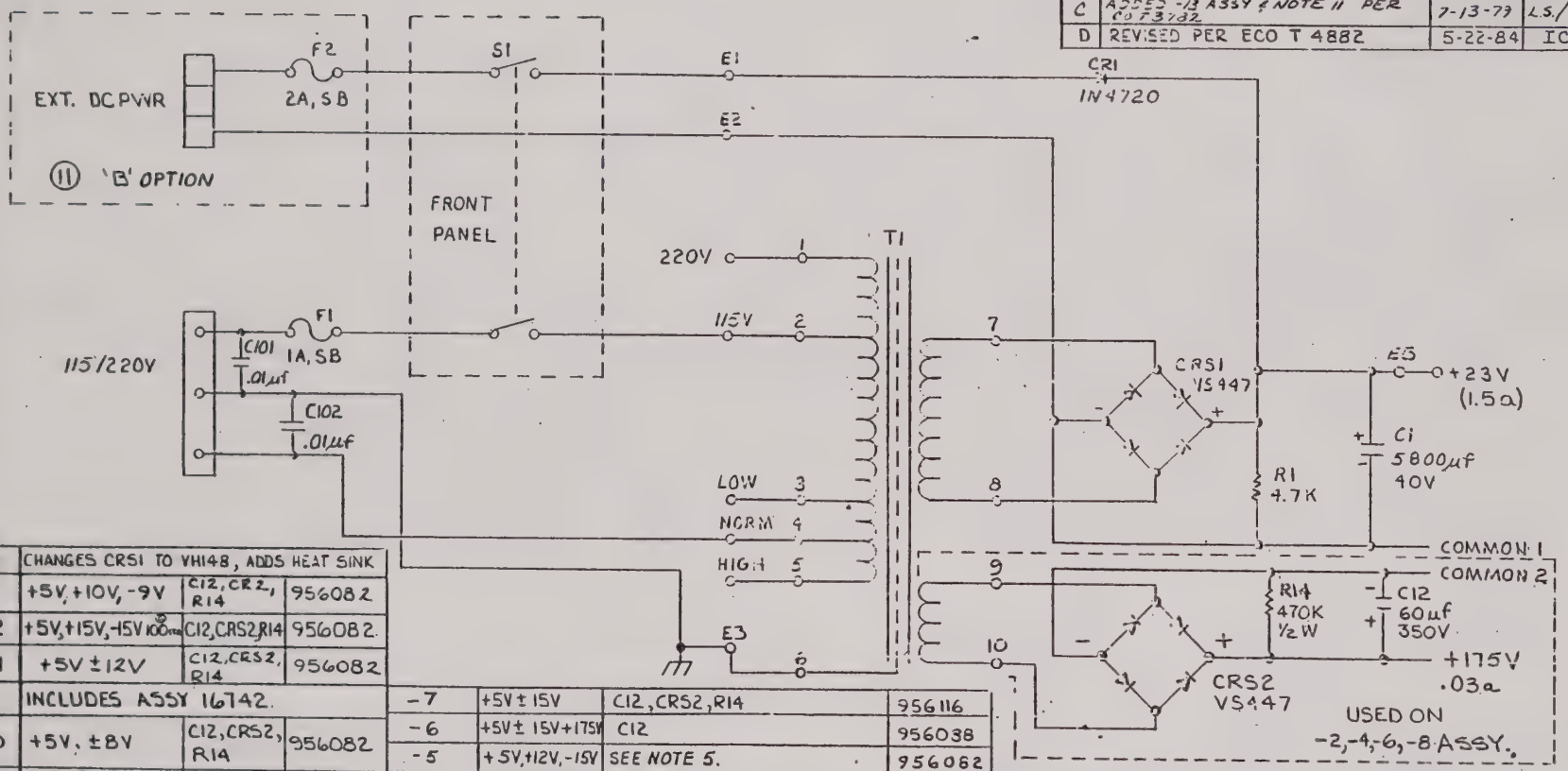
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX = .03
XXX = .010
ANGLES = 1/2°

TITLE
SHAPER MODULATOR
17056

Datum Inc.
170 E. LIBERTY AVE.
ANAHEIM, CALIFORNIA

DWN	DENISE	3/14/81	DES				
CHK			ENGR		A	A-17056	
SCALE	NONE		FSC	31160	SIZE	SHT 1 OF 1	REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
E	REVISED PER ECO T5126	10.3.85	SATINDER
A	C4 WAS 948901 SELECTED 47μf	6-26-73	RM
B	CHANGED A2 PER CO 3576	6-24-77	RM
C	ADDED -13 ASSY & NOTE 11 PER CO F3782	7-13-79	L.S.
D	REVISED PER ECO T 4882	5-22-84	IC



DASH NO		COMP. NOT USED	XFORMER USED
-H	CHANGES CRS1 TO VH148, ADDS HEAT SINK		
-13	+5V, +10V, -9V	C12, CR2, R14	956082
-12	+5V, +15V, -15V 100ma	C12, CRS2, R14	956082
-11	+5V ±12V	C12, CRS2, R14	956082
A	INCLUDES ASSY 16742.		
-10	+5V, ±8V	C12, CRS2, R14	956082
-9	-1, -3, -5, OR -7 USED WITH 16742		
-8	+5V, +12, -15, +175	C12	956088
-7	+5V ± 15V	C12, CRS2, R14	956116
-6	+5V ± 15V + 175V	C12	956038
-5	+5V, +12V, -15V	SEE NOTE 5.	956082
-4	+5V, ±15V, +175V		956088
-3	+5V, ±15V	C12, CRS2, R14	956082
-2	+5V, +175V	A2, A3, C8, C9, C10, C11 CR7, CR8	956088
-1	+5 ONLY	A2, A3, C8, C9, C10, C11, C12, CR7, CRS2, R14, CR8	956082
DASH NO.		COMP'S NOT USED	XFORMER USED

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
FRAC ± 1/32
.XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: POWER SUPPLY (49)

DWN EK 3/23/73 DES 3/30/73
CHK 4/27/73 ENG MJP 6/73
SCALE NONE PSC 31100

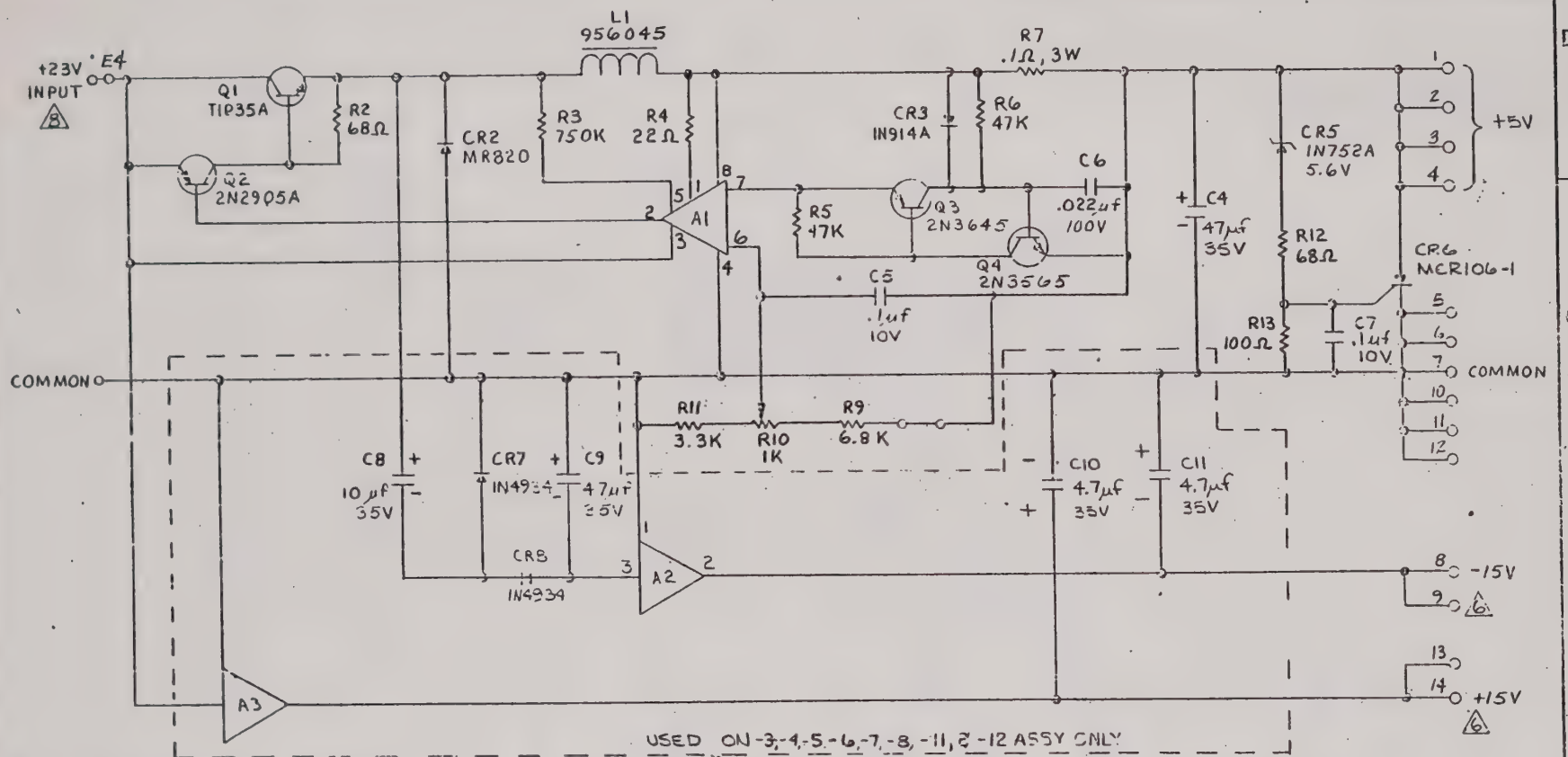
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

B 16280 E

SIZE SHT 1 OF 2

DIETZGEN 1984-10

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



8. +23V OR'ED WHEN -A ASSY USED
7. -10 ASSY A3 IS 7808, A2 IS 79M08
6. -5 & -8 ASSY OUTPUT IS +12V -10 ASSY OUTPUT IS ± 8V
5. -5 ASSY A3 IS UGA7812393 OR MC7812 CP
4. A3 IS UGA7815393 OR MC7815CP
3. A2 IS MC7915CP OR 7915UC
2. A1 IS LM305
1. RESISTORS ARE ¼ W, 5%

NOTES: UNLESS OTHERWISE SPECIFIED

12. -H ASSY: CR51 IS VH148; ADD HEAT SINK.
11. -13 ASSY: A2 IS LM7909CT; A3 IS LM7810CT
10. -12 ASSY: A2 IS 7915UC
9. -11 ASSY: A2 IS MC7912CP, A3 IS MC7812CP

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .03, .XXX ± .010, ANGLES ± 1/2°

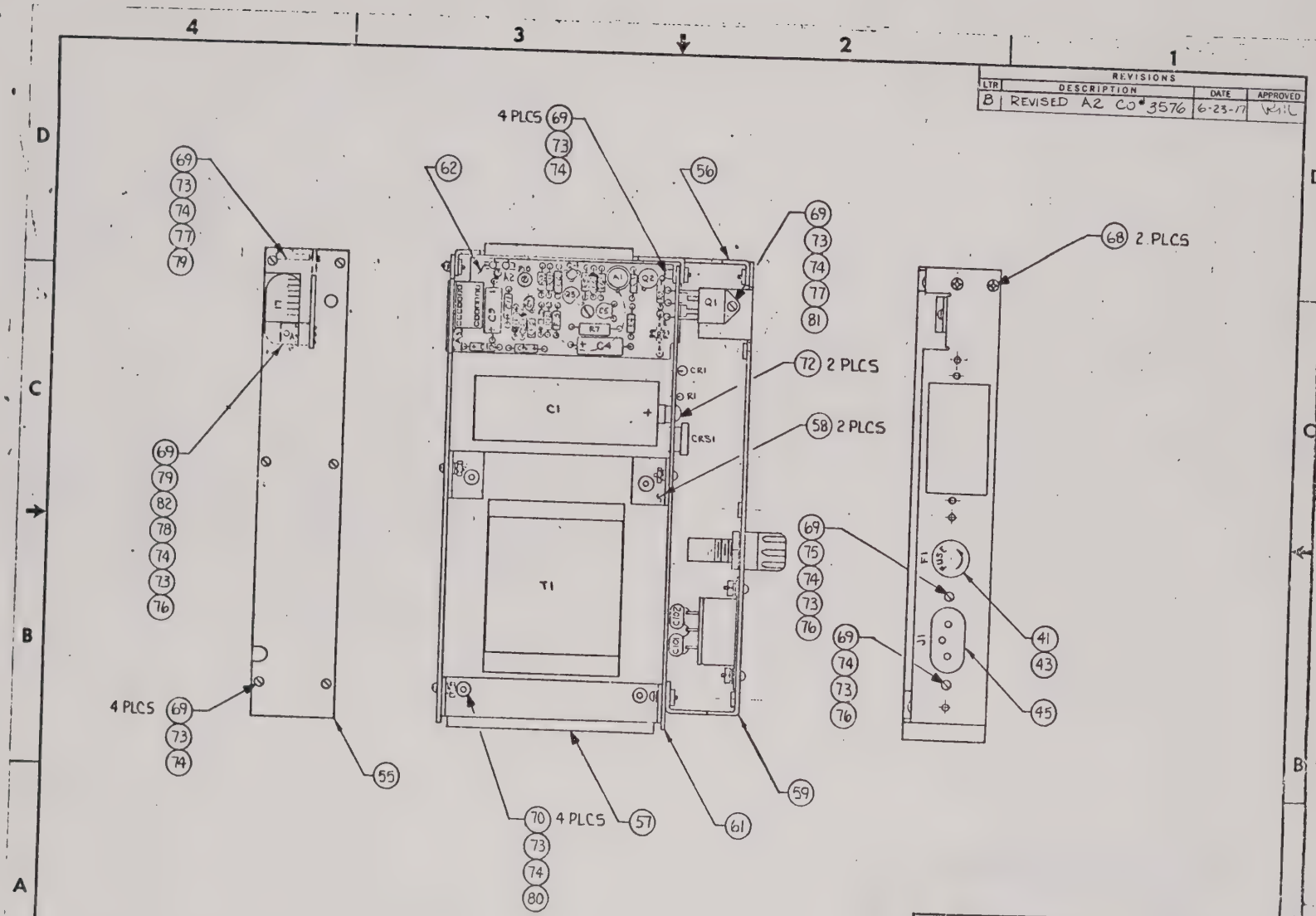
TITLE: REGULATOR (49)

DWN	EK	3/23/73	DES		3/30
CHK			ENGR	MP	6/73
SCALE	NONE	FSC	31160	SIZE	B
				SHT	2 OF 2

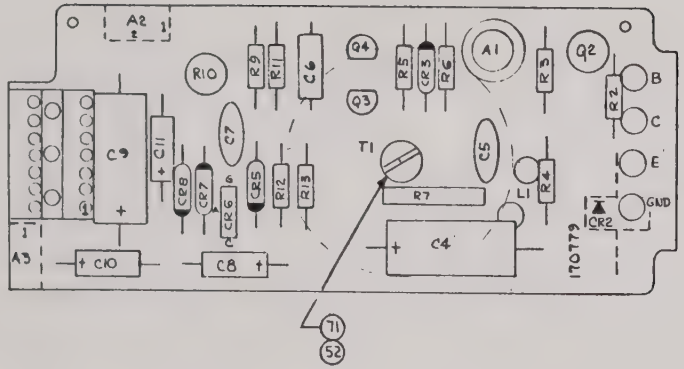
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

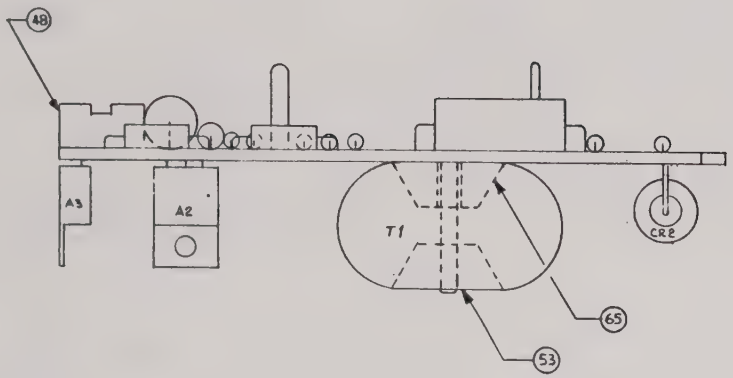
16280

DIETZGEN 1964-10


4
3
2
1
D
C
B
A
REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
B | REVISED A2 CO #3576 | 6-23-17
4 PLCS 69 73 74
62
56
69 73 74 77 81
72 2 PLCS
58 2 PLCS
68 2 PLCS
69 73 74 77 79
69 79 82 78 74 73 76
4 PLCS 69 73 74
55
69 75 74 73 76
41 43
69 74 73 76
45
70 4 PLCS 73 74 80
57
61
59
C1
T1
Q1
Q2
CR1
R1
CRS1
F1
4 AMP
J1
SEE 'C' SIZE FOR SHEET 2
NOTES: UNLESS OTHERWISE SPECIFIED
TITLE
POWER SUPPLY
Datum inc.
370 E. LUCKY AVE.
ANAHEIM, CALIFORNIA
DWN
CHK
ENGR
MFG
APVD
DATE
NONE
31160
B
A-16280
C
SHT 1 OF 2
REV

DESCRIPTION	DATE	APPROVED





SHT 1 OF THIS ASSY IS "B" SIZE

NOTES: UNLESS OTHERWISE SPECIFIED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: ASSEMBLY AID-REGULATOR

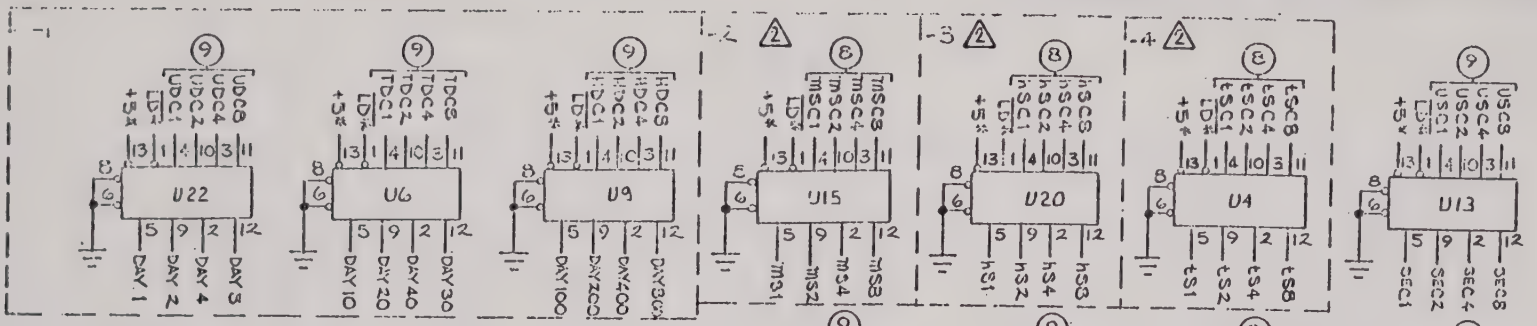
DWN	EM	11/27/78	DES		
CHK			ENGR	WR	
SCALE	2:1		FSC	31160	

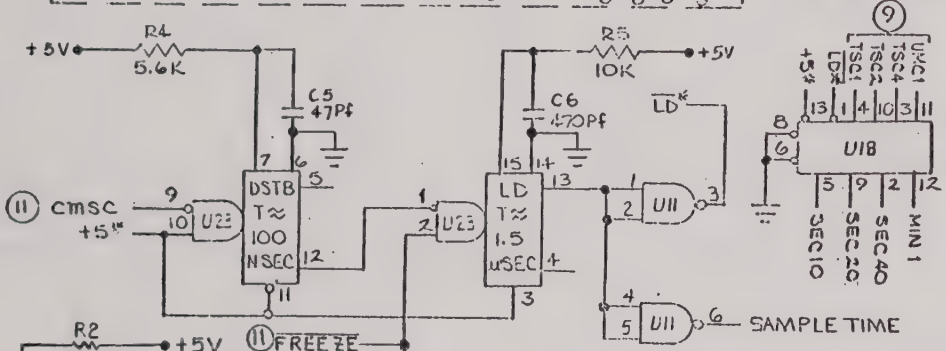
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

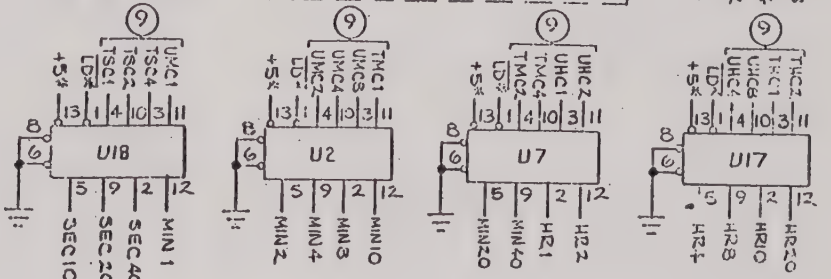
SIZE	DWG NO	REV
C	A-16280-3	C

SHT 2 OF 2

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	REDESIGNED PER ECO T4508	4-21-82	DL
B	ADDED NOTE 2	8-25-82	DL/DR







SN74LS196N	T.I.	U2,4,6,7,9,13,15,17,18,20,22
SN74LS153N		U3,5,8,10,14,16,19,21
SN74LS123N		U23
SN74LS37N		U11
SN74LS08N	T.I.	U1
PART NO.	MFR.	REF. DES.

2 BCD TERMS ORIGINATE ON 13 IF CODE SELECT INSTALLED

1. ALL UNUSED TERMS WILL BE GROUNDED AT 74LS153 INPUTS

-4 ts TERMS
-3 hs TERMS
-2 ms TERMS
-1 DAYS

NOTES: UNLESS OTHERWISE SPECIFIED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

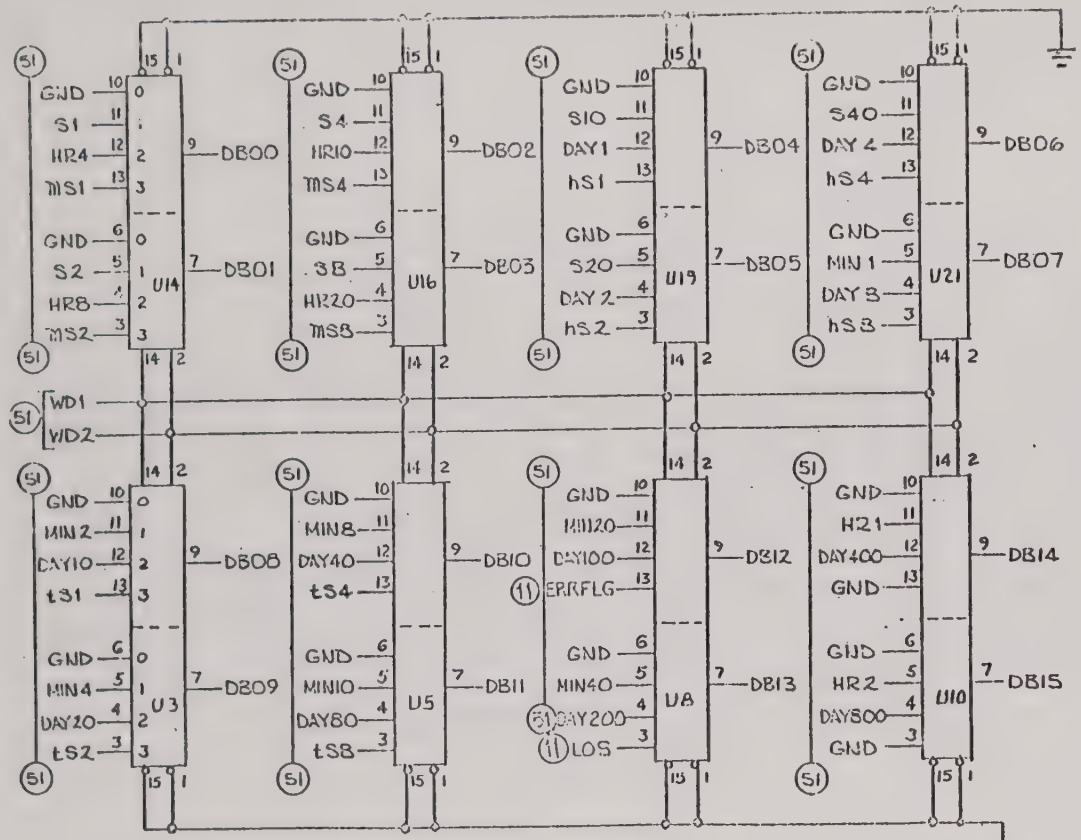
TITLE: S/H REGISTER (LOW POWER) (51)

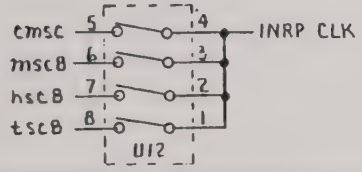
DWN BLS 8/12/76
CHK DR 8/76
SCALE NONE

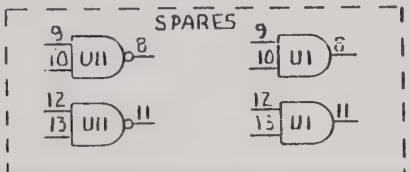
DATUM INC. 11105 SEVEN OAKS BLVD. ANAHEIM, CALIFORNIA 92803

13 16989 B

SHT 1 - 2







L	≤ 0.8 VDC	DATA 2	DATA 1	WORD	TIME
H	≥ 2.4 VDC	L	L	0	ALL OUTPUTS LOW
		L	H	1	HR2 ← → S1
		H	L	2	DAY800 ← → HR4
		H	H	3	mS800 ← → MS1

WORD FORMAT

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	BIT #
	WORD 0
HOURS: UNITS 2 1 — MINUTES: TENS 4 2 1, UNITS 8 4 2 1 — SECONDS: TENS 4 2 1, UNITS 8 4 2 1	WORD 1
DAYS: HUNDREDS 8 4 2 1, TENS 8 4 2 1, UNITS 8 4 2 1 — HOURS: TENS 2 1, UNITS 8 4	WORD 2
LOS, ERROR — MILLISECONDS: HUNDREDS 8 4 2 1, TENS 8 4 2 1, UNITS 8 4 2 1	WORD 3

(52) S/H REGISTER (DATA MULTIPLEXERS)

B 16989 B

SIZE SHT 2 OF 2

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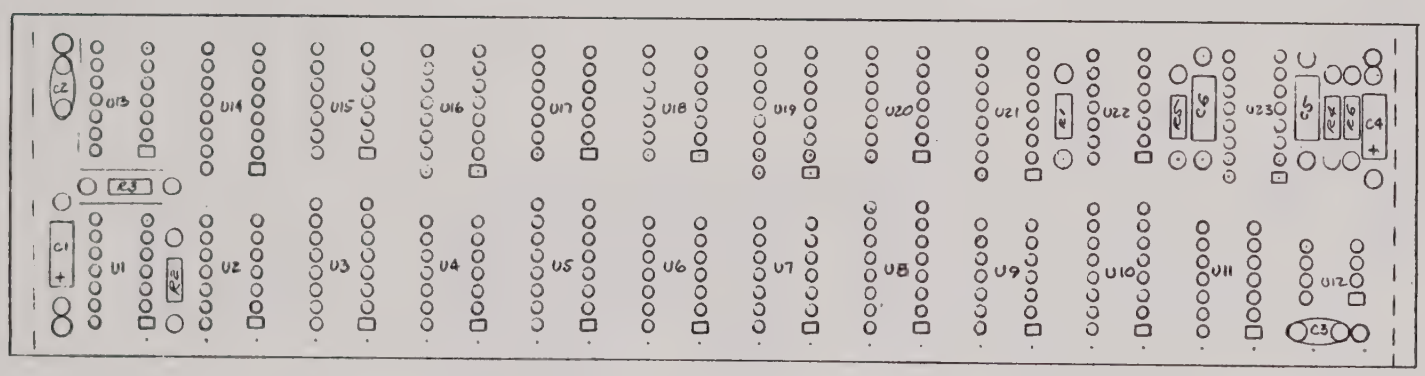
© BUNKER RAMO NIXDORF ACCUPRESS REORDER NO. A0289

LTR	DESCRIPTION	DATE	APPROVED



1. P.C. BOARD 171791

NOTES: UNLESS OTHERWISE SPECIFIED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: .XX ± .02 .XXX ± .005 ANGLES ± 1/2°

TITLE: S/H REGISTER

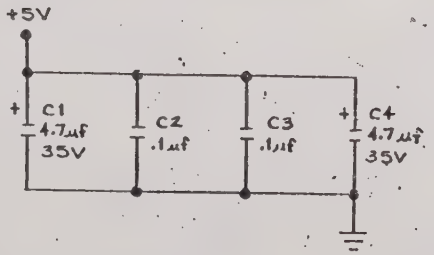
DWN		DES IC	4/8/82
CHK		ENGR	
SCALE 2:1		FSC 31160	

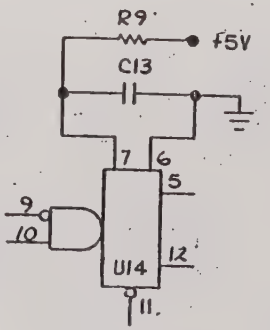
Datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

SIZE		SHT		OF		REV
C	A - 16989	1		1		B

BISHOP GRAPHICS/ALLEGPRESS NEWBURYPORT, MASS.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED





NOT USED

PART NO	MFR	REF
SN74LS123N	T.I.	U9, 14, 19
SN74LS157N		U3, 4, 15
SN74LS00N		U6, 17
SN74LS04N		U7
SN74LS10N		U8
SN74LS14N		U1
SN74LS32N		U16
SN74LS74AN		U18
SN74LS86N		U2, 13
SN74LS197N	T.I.	U5
899-1-R2K	BECKMAN	U12
N7486A	SIGNETICS	U10, 11, 20, 21, 22

NOTES: UNLESS OTHERWISE SPECIFIED

THIS DATA IS CONFIDENTIAL TO SATURN INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

TITLE: I/O CONTROL

Saturn Inc.
1303 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA

LARRY	1/6/81		
NONE		B	18180
		SCALE	1 OF 4

0302 TAB 17131 1

47Ω IN SERIES

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

STB
SETFRZ
SETWD2
SETWD1
RST*
SEQSTB*
U5
U7
U17
FREEZE
WD1*
U8
WD2*
U12-10 +5V
DATN00
U1
U2
DATN00*
U12-11 +5V
DATN01
DATN01*
U12-12 +5V
DATN02
DATN02*
U12-2 +5V
.001
DRVSMP
STB
STB+DRVCD*
U19
R1 20K
C5 330PF
DFLG T≈ 3μSEC
R2 6.8K
C6 330PF
FLG T≈ μSEC
FLG1
U18
+5V
2K
U12-3
C12 .01μf
U12-8 +5V
.001
DATRCVD
DRCVD
U12-1 +5V
RESET
RST
POL
E3
GND. TRUE
POS. TRUE
E1
E2
DATA POLARITY SELECT
DRCVD*
U16
U10
FLGDC
U11
FLGPULSE
FLAG

1. ALL RES. ARE 2K (RES. PACK)
NOTES: UNLESS OTHERWISE SPECIFIED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

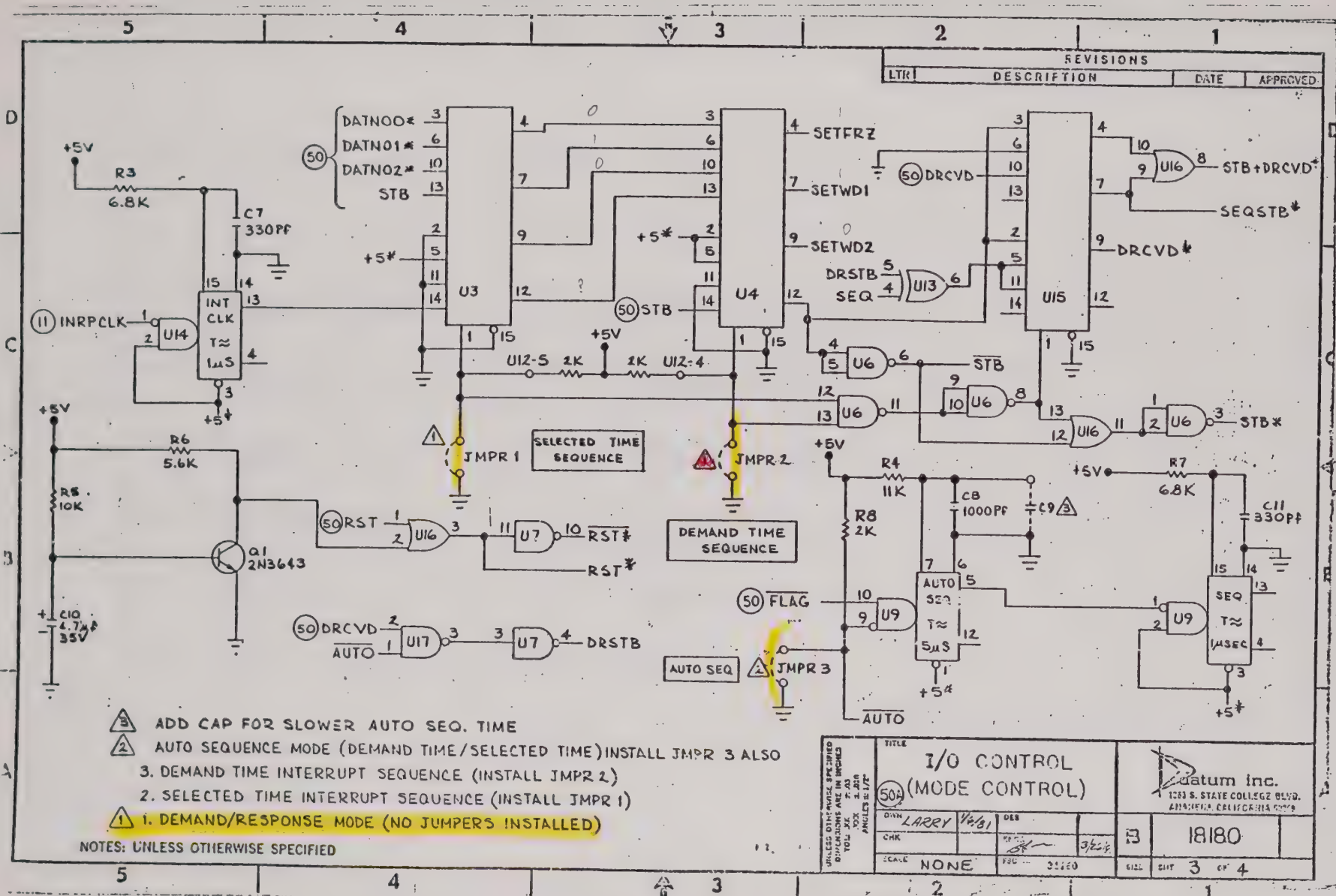
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: X ±.03 XX ±.010 ANGLES ± 1/2°

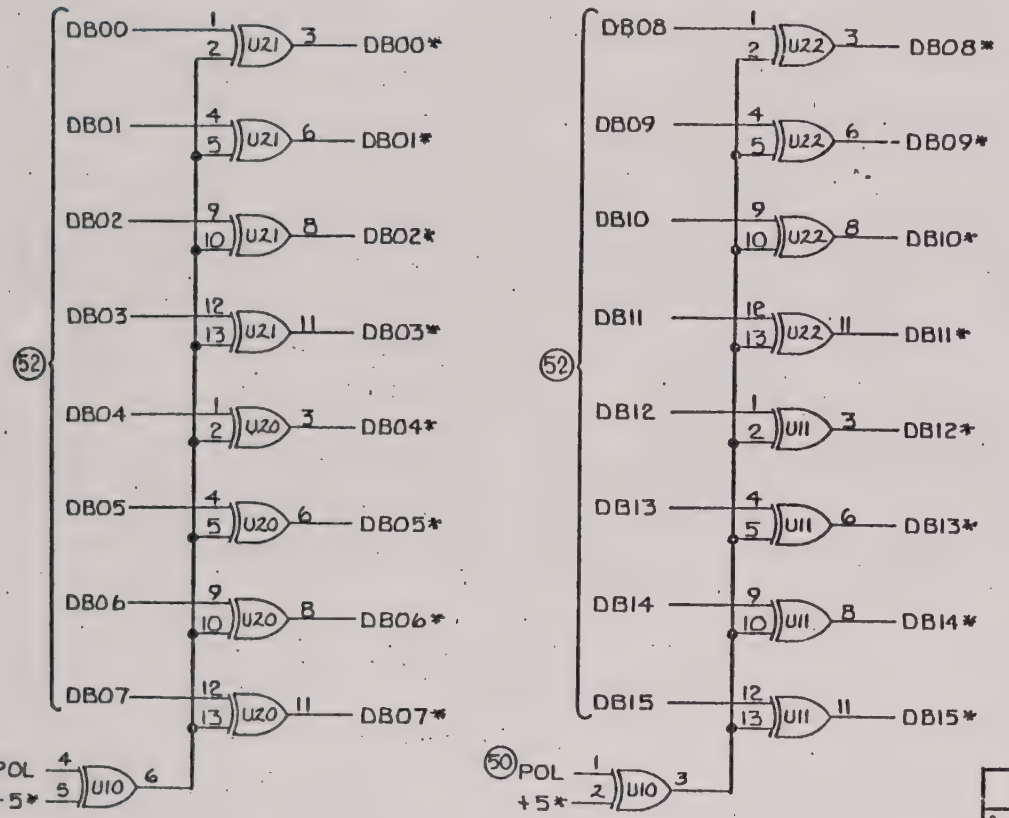
TITLE
I/O CONTROL
(DATA CONTROL)
50

Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM CALIFORNIA 92806

DRN	LARRY	1/16/81	DES			
CH			ENG			
SCALE	NONE		MFG	21160	SIZE B	18180
					SHT 2 OF 4	

Check with MFG


REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
DATNO0*
DATN01*
DATN02*
STB
SETFRZ
SETWD1
SETWD2
DRSTB
SEQ
DRCVD
STB+DRCVD*
SEQSTB*
DRCVD*
INRPCLK
INT CLK T≈ 1μS
U3
U4
U13
U15
U16
U6
U14
U12-5
U12-4
2K
R3 6.8K
C7 330PF
R6 5.6K
R5 10K
Q1 2N3643
C10 4.7μF 35V
R4 11K
R8 2K
C8 1000PF
C9
R7 6.8K
C11 330PF
JMPR 1
SELECTED TIME SEQUENCE
JMPR 2
DEMAND TIME SEQUENCE
JMPR 3
AUTO SEQ
RST
RST*
U17
U7
DRSTB
FLAG
U9
AUTO SEQ T≈ 5μS
SEQ T≈ 1μSEC
AUTO
ADD CAP FOR SLOWER AUTO SEQ. TIME
AUTO SEQUENCE MODE (DEMAND TIME/SELECTED TIME) INSTALL JMPR 3 ALSO
3. DEMAND TIME INTERRUPT SEQUENCE (INSTALL JMPR 2)
2. SELECTED TIME INTERRUPT SEQUENCE (INSTALL JMPR 1)
1. DEMAND/RESPONSE MODE (NO JUMPERS INSTALLED)
NOTES: UNLESS OTHERWISE SPECIFIED
TITLE
I/O CONTROL
(MODE CONTROL)
DWN LARRY 1/26/81
CHK
SCALE NONE
Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA
SIZE B
18180
SHT 3 OF 4



NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOL: XX ± .03, .XXX ± .010, ANGLES ± 1/2°

TITLE: I/O CONTROL (DATA OUTPUTS)

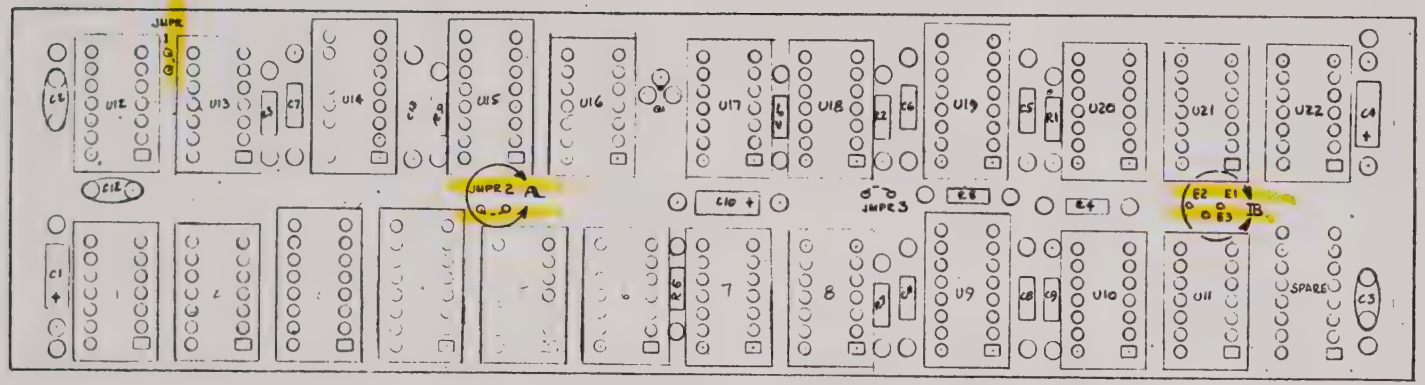
508

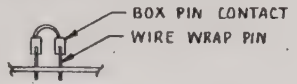
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA

DWN	LARRY	1/6/81	DES		
CHK			ENGR		
SCALE	NONE		FSC	31160	SIZE B

18180

SHT 2 OF 4





DETAIL A
(TYPICAL 3 PLC'S)

DETAIL IB

P.C.I 171726

NOTES: UNLESS OTHERWISE SPECIFIED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: I/O CONTROL

Datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

DWN	IC	11/5/81	DES	IC	11/5/81
CHK			ENGR		
SCALE	2:1		FSC	31160	

C | A-18160 | SHT 1 OF 1 | REV

SECTION VII
LIST OF MATERIALS

The following terms are used on the materials lists form. Their specific usage is explained below to aid in using the included information for replacement part logistics.

a. ITEM — A numeric listing of each part or component comprising each assembly.

b. STOCK/PART Number -- Each part or component is identified by its DATUM stock number or original manufacturer's part number. A DATUM stock number is used when the part is maintained in DATUM's stock inventory. The manufacturer's part number is used when the part is not maintained in inventory.

c. DESCRIPTION -- Each part or component is identified by its descriptive nomenclature.

d. MFR/SPEC —Each part or component availability source is listed. Those items identified with DATUM stock numbers show "DATUM". Those not in inventory (and listed by original manufacturer's part number) show the original manufacturer.

e. QTY — The quantity of each item utilized in the assembly.

f. REF. DES. —Identification of the part or component as indicated on the support schematic drawing.

g. UNIT COST, LOT TOTAL —For customer use, as desired.

1.	Time Code Generator/Translator	9300-7323
2.	AGC	16085
3.	NASA Decoder	16446-156
4.	LED Display	16447-1
5.	Shaper Modulator	17056
6.	Power Supply	16280-3
7.	S/H Register	16989-1234
8.	I/O Control	18180

DATE: 2-17-84
DRAWN: CAD4
CHK:

MATERIAL LIST

TITLE: TIME CODE GEN/TRANS

datum inc.

JOB NO:
QUANTITY

REV

ASS'Y NO: 9300-7323

SHT 1 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	SK9100-2	SHIPPING KIT	DATUM	1			
2							
3	0226-0104-1	CAPACITOR .1μf		1			
4							
5	1202-0102	SWITCH SPDT		4			
6	1204-3903	" P/B		10			
7	1206-9634	" ROTARY		1			
8	1212-7606-1	" T/W		1			
9	1299-765G-1	BAND HOWE		1			
10							
11	1704-0036	CONNECTOR 36P		1			
12	" -1002	" BNC		2			
13	" -1625-6R	" 6P		1			
14	1708-3897	SOCKET 14P W/W		2			
15	" -3898	" 16P "		1			
16	1792-1561	CONTACT, SOCKET		6			
17	1795-0001	WASHER		2			
18	" -0002	"		2			
19							
20	2325-2005	FASTENER		2			
21							
22	2524-5010	KNOB		1			
23							
24	170296 N/C	PC BOARD STK		1			
25	170979A	" " STK		1			
26							

NOTES:

DATE: 2-17-84
DRAWN: CARY
CHK:

MATERIAL LIST

datum inc.

TITLE: TIME CODE GEN/TRANS

JOB NO:
QUANTITY
ASS'Y NO: 9300-7323

REV

SHT 2 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
27	700362	CENTER SUPPORT STK	DATUM	1			
28	700364-2	COVER STK		2			
29	700546	STIFFENER STK		6			
30	703335-2	BUTCH PLATE STK		1			
31	703995	MTG BRKT STK		2			
32	704757-2	SIDE GUSSET STK		2			
33	704899-1	REAR PANEL STK		1			
34	705850	FRONT PANEL STK		1			
35	705853	COVER PLATE STK		1			
36	705866-3	LENS STK		1			
37	707349-1	BUTCH PLATE STK		1			
38	703336	CONN PLATE STK		1			
39	931500	HANDLE STK		2			
40							
41	16085	AGC STK		1			
42	16280-3	POWER SUPPLY STK		1			
43	16446-156	NASA DECODER		1			
44	16447-1	DISPLAY		1			
45	17056	SHAPER MOD		1			
46	16989-1234	SAMPLE/HOLD REG STK		1			
47	18180	I/O CONTROL STK		1			

NOTES:

DATE: 3-6-73
DRAWN: GHC
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY:

TITLE: AGC

ASS'Y NO: 16085

H

1 of 3

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.
1	0102-0330	RESISTOR 33Ω 1/4W 5%	DATUM	1	R10
2	" -0910	" 91Ω " "	"	1	R3
3	" -0391	" 390Ω " "	"	1	R44
4	" -0511	" 510Ω " "	"	1	R18
5	" -0561	" 560Ω " "	"	1	R17
6	" -0102	" 1K " "	"	7	R21,22,26,33,38,43,45
7	" -0122	" 1.2K " "	"	1	R37
8	" -0152	" 1.5K " "	"	1	R30
9	" -0202	" 2K " "	"	1	R46
10	" -0272	" 2.7K " "	"	3	R25,32,39
11	" -0302	" 3K " "	"	1	R31
12	" -0512	" 5.1K " "	"	8	R4,8,12-14,20,34,40
13	" -0682	" 6.8K " "	"	1	R29
14	" -0752	" 7.5K " "	"	1	R16
15	" -0103	" 10K " "	"	7	R5-7,11,28,36,41
16	" -0183	" 18K " "	"	1	R24
17	" -0473	" 47K " "	"	1	R23
18	" -0753	" 75K " "	"	1	R19
19	" -0124	" 120K " "	"	4	R2,9,15,35
20	" -0274	" 270K " "	"	1	R47
21	" -0105	" 1M " "	"	3	R1,27,42
22	C104-0221	" 220Ω 1/2W "	"	1	R48
23					
24	0220A74	CAPACITOR .47Mf 35V	"	2	C4,8
25	" -0105	" 1Mf "	"	6	C2,15,16,19-21
26	" -0475	" 4.7Mf "	"	5	C3,12,13,17,18

NOTES:

DATE: 3-6-75
DRAWN: GHC
CHK:

MATERIAL LIST

Datum inc.

JOB NO:
QUANTITY:
TITLE: AGC
ASS'Y NO: 16085

H

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.
27	0220-0107	CAPACITOR 100Mf 10V	DATUM	1	C14
28	0221-0221	" 220Mf 4V	"	2	C11A, 11B
29	0225-0471	" 470Pf	"	1	C12
30	" -0152	" 1500Pf	"	1	C10
31	0226-0100	" 10Pf	"	1	C6
32	" -0470	" 47Pf	"	1	C9
33	" -0103-1	" .01Mf 100V	"	1	C7
34	" -0203	" .02Mf "	"	1	C5
35	" -0104-1	" .1Mf "	"	1	C1
36					
37	0301-7405	FC N7405A	"	1	A5
38	" -7749	" N6A7749393	"	2	A1,4
39	" -9311-H	" LM311H	"	2	A2,3
40					
41	0500-0306	DIODE 1N914A	"	2	CR1,3
42	0515-0705-1	" 1N705A	"	1	CR2
43	" -0752-1	" 1N752A	"	1	CR4
44					
45	0550-7705	TRANSISTOR 2N3565	"	1	Q6
46	0555-6600	" 2N3645	"	1	Q7
47	0570-1087	" P1087E	"	3	Q3-5
48	" -8703	" U1487E	"	1	Q2
49	" -8704	" 988704	"	1	Q1
50					
51					
52					

NOTES:

DATE: 3-6-75
DRAWN: RAE
CHK:

MATERIAL LIST

datum inc.

JOB NO.
QUANTITY:

TITLE: AGC

ASS'Y NO. 16085

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.
53	1708-3100-1	SOCKET 14P	DATUM	3	
54	" -8000	" 8P	"	2	
55					
56	170574-E1	PC BOARD STK	"	1	
57	170785-MK	" STK	"	1	

NOTES:

DATE: 12-17-76
DRAWN: R. FLOCK
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY
REV G
TITLE: NASA 36 BASIC
ASS'Y NO: 16446-156
SHT 1 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.				REF. DES.	UNIT COST	LOT TOTAL	
1	0102-0221	RESISTOR, 220Ω, 1/4W, 5%	DATUM	1				R21			
2	" -0102	" 1K " "	"	3				R7,8,9			
3	" -0202	" 2K " "	"	6				R3,4,5,10,11,15			
4	" -0512	" 5.1K " "	"	1				R20			
5	" -0562	" 5.6K " "	"	4				R1,2,13,14			
6	" -0333	" 33K " "	"	2				R6,12			
7											
8	0220-0475	CAPACITOR 4.7uf @35V	"	9				C2,3,7,9,11,13,15,16,18			
9	0225-0681	" 680pf @100V	"	1				C6			
10	" -0102	" 1000pf "	"	1				C5			
11	0226-0104	" .1uf @ 10V	"	5				C8,10,12,17,19			
12											
13	0301-7H03	I.C. SN74H103N	"	3				F7, H2, J8			
14	" -7121	" SN7412IN	"	1				E7			
15	" -7123	" SN74123N	"	2			*	D5, H5			
16	" -7151	" SN74151N	"	2			*	E6, H9			
17	" -7153	" SN74153N	"	5			*	E1-E5			
18	" -7157	" SN74157N	"	1			*	H4			
19	" -7192	" SN74192N	"	1			*	D8			
20	" -7194	" SN74194N	"	1			*	J3			
21	" -7400	" N7400A	"	3				D7, F5, J6			
22	" -7404	" N7404A	"	2				F4, J4			
23	" -7408	" N7408A	"	8				D3,4, E8, F6,8, H1,7,8			
24	" -7420	" N7420A	"	1				H3			
25	" -7432	" SN7432N	"	4				F1-3, H6			
26	" -7442	" N7442B	"	1			*	D6			

NOTES:

DATE: 12-17-76
DRAWN: R. FLOCK
CHK:

MATERIAL LIST

TITLE: NASA 36 BASIC

datum inc.

JOB NO:
QUANTITY
ASS'Y NO: 1646-156

REV G
SHT 2 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.				REF. DES.	UNIT COST	LOT TOTAL
27	0301-7447	I.C. N7447B	DATUM	9			*	B1-9		
28	" -7474	" SN7474N	"	2				J1,7		
29	" - 7486	" N7486A	"	1				J5		
30	" - 8280	" N8280A	"	12				C1-3,5,7-10, D1,2,9,10		
31	" - 8281	" N8281A	"	2				J2,9		
32	" - 8288	" N8288A	"	2				C4,6		
33										
34	1301-0001	OSCILLATOR 1MHz	"	1						
35										
36	1708-3897	SKT 14P W/W	"	50						
37	" -3898	" 16P "	"	22			*			
38	2310-1591-B	MTG BLOCK	"	2						
39	170936 C	P.C. BD STK	"	1						
40										
41	0126-R220-2	RESISTOR CHIP 220Ω	"	9				A1-9		

NOTES:

DATE: 4-10-75
DRAWN: RHE
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY
REV

TITLE: LED DISPLAY
ASS'Y NO: 16447-1
SHT 1 OF 1

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	1708-0036	HEADER	DATUM	2			
2							
3	" - 3788	SOCKET	"	9			
4							
5	2205-0006	LED DISPLAY	"	9	DS1-9		
6							
7	170937 B	PC BOARD STK	"	1			

NOTES:

DATE: 12-16-76
DRAWN: R. FLOCK
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY

REV A

TITLE: SHAPER MODULATOR

ASS'Y NO: 17056

SHT 1 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
1	0102-0100	RESISTOR, 10Ω, 1/4W, 5%	DATUM	2	R26,27		
2	" -0510	" 51Ω " "	"	1	R25		
3	" -0102	" 1K " "	"	3	R28,30,31		
4	" -0222	" 2.2K " "	"	1	R13		
5	" -0332	" 3.3K " "	"	1	R3		
6	" -0472	" 4.7K " "	"	1	R12		
7	" -0103	" 10K " "	"	5	R2,11,16,18,19		
8	" -0473	" 47K " "	"	3	R6,10,14		
9	" -0104	" 100K " "	"	1	R20		
10	0115-2052	" 20.5K " 1%	"	1	R8		
11	" -2262	" 22.6K " "	"	3	R4,5,9		
12	0154-5001	POT 5K	"	3	R7,15,17		
13							
14	0212-0222	CAPACITOR .0022uf@100V	"	2	C6,8		
15	" -0223	" .022uf "	"	2	C7,9		
16	0220-0475	" 4.7uf @35V	"	3	C1,3,5		
17	0225-0221	" 220pf @100V	"	1	C10		
18	0226-0104	" .1uf @ 10V	"	4	C2,4,11,12		
19							
20	0301-5558	I.C. N5558V	"	2	A17,18		
21	" -7400	" N7400A	"	1	A15		
22	" -7408	" N7408A	"	1	A16		
23	" -7432	" SN7432N	"	1	A8		
24	" -7486	" N7486A	"	1	A7		
25							
26							

NOTES:

DATE: 12-16-76
DRAWN: R. FLOCK
CHK:

MATERIAL LIST

datum inc.

JOB NO:
QUANTITY

REV A

TITLE: SHAPER MODULATOR

ASS'Y NO: 17056

SHT 2 OF 2

ITEM	STOCK/PART NO.	DESCRIPTION	MFR/SPEC	QTY.	REF. DES.	UNIT COST	LOT TOTAL
27	0570-1087	TRANSISTOR P1087E	DATUM	1	Q1		
28							
29	1706-2010	TERMINAL	"	2	TP1, 3		
30							
31	1708-3897	SKT 14P W/W	"	4			
32							
33	170924 N/C	P.C. BD. STK	"	1			
35	803762	WIRELIST	DATUM	REF.			

NOTES:

INTRODUCTION

This option description provides operational and functional explanations of the 16-bit general purpose interface circuit which has been added to the basic instrument. The output data format, modes of operation and operation are described in Section I of this option description.

GENERAL DESCRIPTION

This circuit provides the ability to transfer timing data to 16-bit parallel, byte serial computer interfaces in a variety of operational modes and with a variety of interface structures. For example, the DEC DR11C/DRV11, the H.P. 12566B, the Data General 4040/4041 and other similar interfaces may be serviced by appropriate use of the available control lines.

Five modes of operation are available with this interface. Each of these modes is described briefly below. For a more detailed description of the operation of each mode, refer to Section I of this option description. Depending upon the limitations of the specific interface being used, not all modes are usable with all interfaces.

1. Demand/Response Mode:
   This mode allows, upon demand, for transfer of all three bytes of the time word or of any one or two of the bytes in any sequence during a data exchange.

2. Demand Time Interrupt Sequence Mode:
   Upon computer demand, this mode sequentially outputs all three time word bytes with the computer controlling the byte output rate.

3. Demand Time Automatic Sequence Mode:
   Upon computer demand, this mode sequentially outputs all three time word bytes with the interface controlling the byte output rate.

4. Selected Time Interrupt Sequence Mode:
   This mode sequentially outputs all three time word bytes following each time word's least significant bit update with the computer controlling the byte output rate.

5. Selected Time Automatic Sequence Mode:
   This mode sequentially outputs all three time word bytes following each time word's least significant bit update with the interface controlling the byte output rate.

The interface may be configured to operate with either positive-true (+5V) or negative-true (ground) TTL-level inputs and outputs.

OPERATING CONTROLS

Mode selection and input/output data polarity control is accomplished with a set of jumpers on the I/O Control circuit card. Four jumpers are provided: one for dasta polarity and three for mode selection. Refer to the Operational Programming paragraph for mode selection. Unless otherwise specified by the customer, when shipped from the factory the interface was configured for positive-true data polarity and for the demand/response mode of operation.

OPERATION

In the following text, raising a data line signifies the active condition. The actual level is dependent upon the selected data polarity. Figures 1 and 2 show the timing relationships of typical interfaces. The data format is shown in Figure 3.

NOTE

The characteristics of all timeout events and flag signals are defined by non-precision components. Therefore, specified values are nominal and are subject to considerable variation.

Demand/Response Mode

The time word is placed in the static condition when the DATN00 (data storage) and DVCMD (strobe) lines are raised. The states of byte-select lines DATN01 and DATN02 determine which byte will be placed on-line in the following manner:

DATN02	DATN01	BYTE
0	1	1
1	0	2
1	1	3

A strobe pulse is required for each byte, and the data storage line must remain high for the duration of the data transfer. The three control lines must remain static as long as the strobe line is raised.

Three microseconds after the strobe line is lowered, the FLG PULSE and FLG DC flag outputs are issued, signifying that valid data in on-line and ready for transfer. The FLG PULSE flag is 1 microsecond in duration. The FLG DC flag remains raised until the acknowledge input (DATRCVD) is received, or until the end of the data exchange if no acknowledge input is available from the interface. The data exchange can be terminated by lowering all three control lines (DATN00, DATN01, and DATN02) and providing a strobe. The time word will then be allowed to update (no flags will be raised).

Demand Time Interrupt Mode

NOTE

This mode of operation requires an interface capable of supplying an acknowledge output after each data byte is accepted.

The time word is placed in the static condition and the first byte is placed on-line when the DVCMD strobe is raised. Three microseconds after the strobe is lowered, the FLG PULSE and FLG DC flags are raised to signify that valid data is on-line. The FLG PULSE flag is 1 microsecond in duration. The FLG DC flag remains raised until the acknowledge input (DATRCVD) is raised. When the acknowledge input is lowered, the second byte is placed on-line. Three microseconds later, the two flag outputs are again issued. Receipt of the second acknowledge input places the third byte on-line and the flag outputs are again issued. Termination of the data transfer will occur upon receipt of the third acknowledge input, and the time word will again be allowed to update.

Demand Time Automatic Sequence Mode

The time word is held in the static condition and the first word is placed on-line when the DVCMD strobe is produced. Three microseconds after the strobe line is lowered, the FLG PULSE and FLG DC flags are issued to signify that data is on-line. the FLG PULSE flag is 1 microsecond in duration, and FLG DC is 5 microseconds long. The second byte is placed on-line 1 microsecond following termination of FLG DC, then both flags are produced again after another 3 microseconds have elapsed. After an additional 5 microseconds, FLG DC is terminated again. The third byte is placed on-line 1 microsecond later, followed in 3 microseconds by the third set of flag outputs. Approximately 5 microseconds later, FLG DC is again terminated, the data transfer is completed and the time word is again allowed to update.

The 5-microsecond nominal duration of the FLG DC flag can be altered by adjusting the time constant of the Auto Sequence one-shot on the I/O Control Assembly. This is accomplished by installing the appropriate capacitor in accordance with the component manufacutrer's recommendations.

Selected Time Interrupt Mode

This mode is similar to the Demand Time Interrupt Mode, except that a data transfer is initiated by the timing instrumentation at the least sifnificant bit (LSB) update rate (usually one millisecond). The first byte is automatically placed on-line when the time update occurs. Four microseconds later the first flag outputs are produced. Subsequent operation is as described in the Demand Time Interrupt Mode paragraph. In this mode, data transfer must be completed prior to the next LSB update.

Selected Time Automatic Sequence Mode

This mode is similar to the Demand Time Automatic Sequence Mode, except that data transfer is initiated by the timing instrumentation at the least significant bit update rate

(usually one millisecond). The first byte is placed on-line when the time update occurs. Four microseconds later the first flag outputs are produced. Subsequent operation is as described in the Demand Time Interrupt Mode paragraph.

Operational Programming (I/O Control Assembly)

1. Data Polarity

   A Box-Pin jumper is provided near IC location U11 to select the "true" TTL input/output logic levles.

   Positive True: E2 to E3

   Negative True: E1 to E3

2. Operating Mode

   1) Demand Response - No Jumpers
   2) Selected Time Interrupt Sequence - Jumper 1
   3) Demand Time Interrupt Sequence - Jumper 2
   4) Selected Time Automatic Sequence - Jumpers 1 and 3
   5) Demand Time Automatic Sequence - Jumpers 2 and 3

Interface Connections

The attached Timing Diagrams and Wiring Diagrams illustrate the operational differences and the lines used with the respective interfaces and applicable modes.

DEC DR11-K Interface

1. GENERAL

   When operating with a DR11-K interface, the DATUM I/O Control assembly must be set up for "GND" true logic. This is easily accomplished by moving the "box pin" jumper from E2 (positive true) to E1 (gnd true).

2. OUTPUT CONTROL WORD

   As seen from the previous I/O description, the "control word" via the DR11-K output register is in the "low" byte (OUT00, 01, 02) and the DR11-K should be programmed accordingly (either LOAD LOW BYTE or LOAD OUTPUT REGISTER may be used).

   The OUTPUT FLAG pulse (FLG. PULSE) is tied back to the DR11-K (EXT DATA ACC/status bit 15) to indicate that the output control word was received. Generally, this line can be ignored except as a double check since the FLGDC line (EXT DATA RDY/status bit 07) is occurring simultaneously indicating that the "time data" word is ready to be input.

3. INPUT TIME WORD

As stated in the above paragraph, the response to the control word output is FLGDC (EXT DATA RDY/status bit 07) indicating that the time data word (See word format in following pages) is ready to be input to the DR11-K.

When the data is read into the computer, the resulting INT DATA ACC signal from the DR11-K causes the FLGDC signal to be reset and conditions the I/O Control for the next output control word.

DEC DR11-K INTERFACE

1. GENERAL

When operating with a DR11-K interface, the DATUM I/O Control assembly must be set up for "GND" true logic. This is easily accomplished by moving the "box pin" jumper from E2 (positive true) to E1 (gnd true).

2. OUTPUT CONTROL WORD

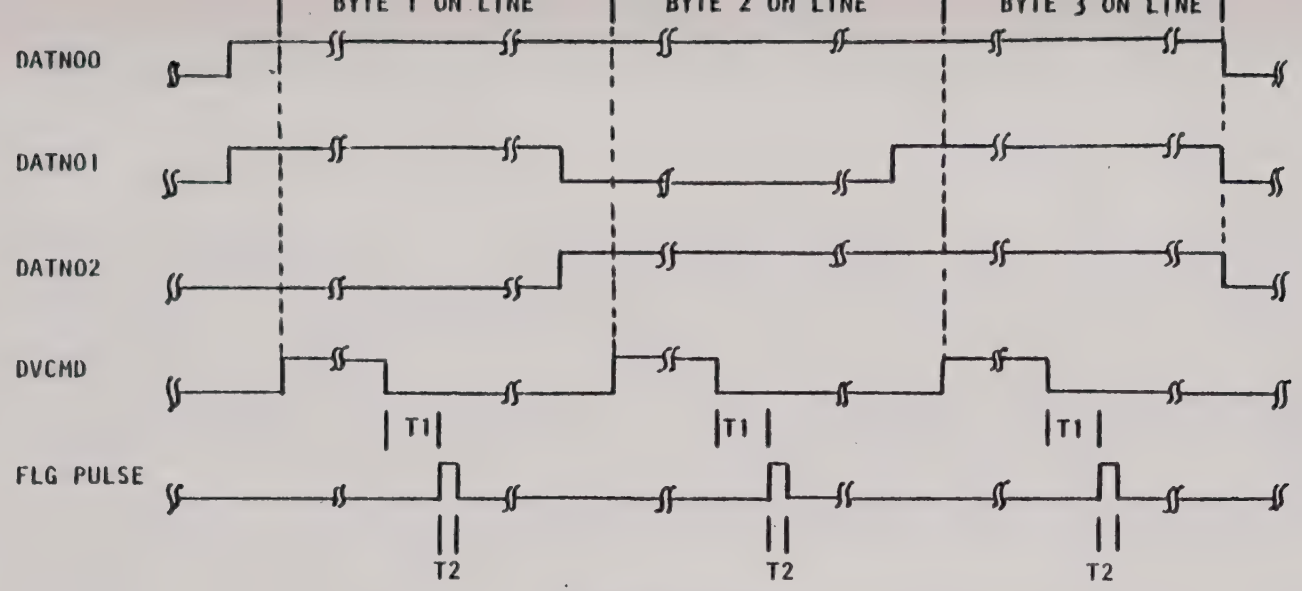
As seen from the previous I/O description, the "control word" via the DR11-K output register is in the "low" byte (OUT00, 01, 02) and the DR11-K should be programmed accordingly (either LOAD LOW BYTE or LOAD OUTPUT REGISTER may be used).

The OUTPUT FLAG pulse (FLG PULSE) is tied back to the DR11-K (EXT DATA ACC/status bit 15) to indicate that the output control word was received. Generally, this line can be ignored except as a double check since the FLGDC line (EXT DATA RDY/status bit 07) is occurring simultaneously indicating that the "time data" word is ready to be input.

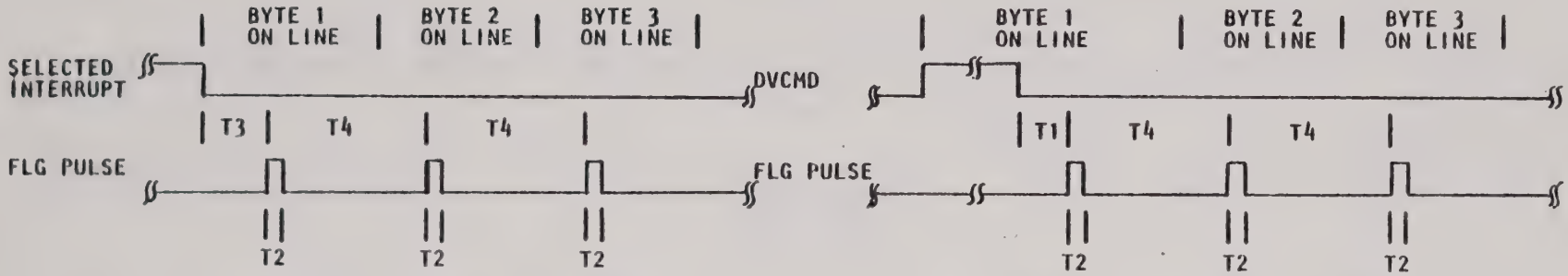
3. INPUT TIME WORD

As stated in the above paragraph, the response to the control word output is FLGDC (EXT DATA RDY/status bit 07) indicating that the time data word (See word format in following pages) is ready to be input to the DR11-K.

When the data is read into the computer, the resulting INT DATA ACC signal from the DR11-K causes the FLGDC signal to be reset and conditions the I/O Control for the next output control word.



DEMAND/RESPONSE

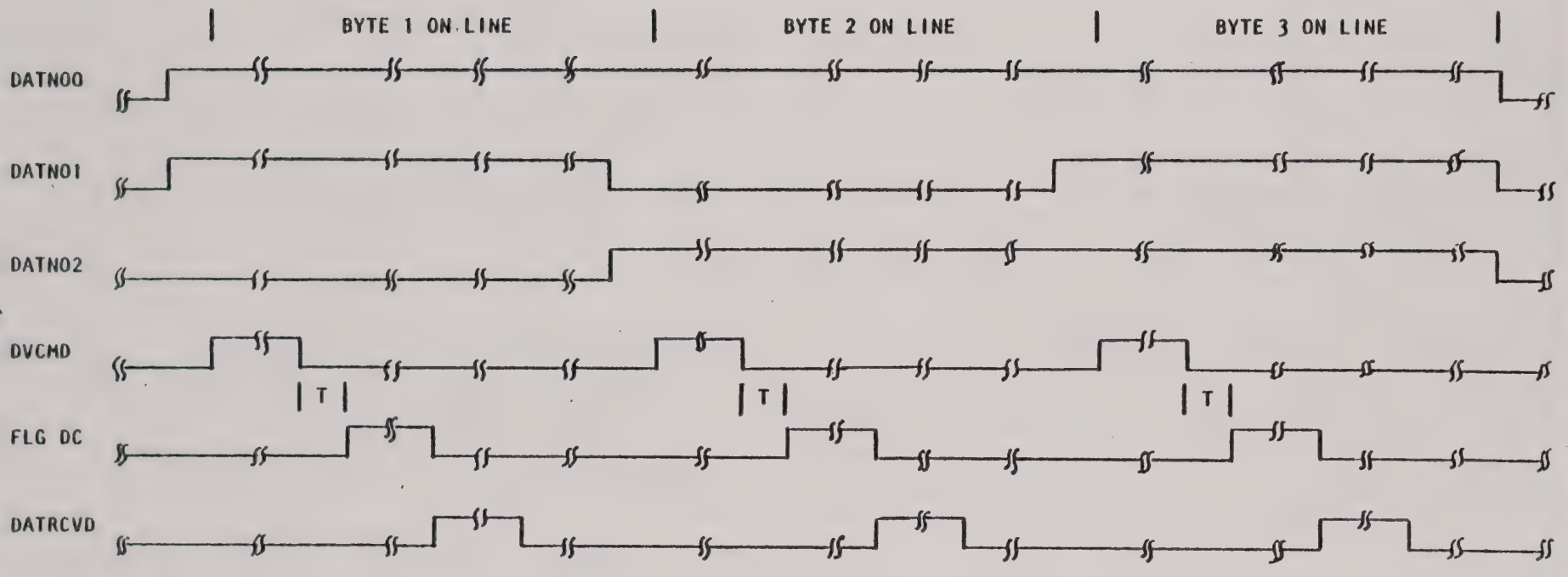


SELECTED TIME AUTOMATIC SEQUENCE

DEMAND TIME AUTOMATIC SEQUENCE

T1--Approximately 3 Microseconds
T2--Approximately 1 Microsecond
T3--Approximately 4 Microseconds
T4--Approximately 10 Microseconds

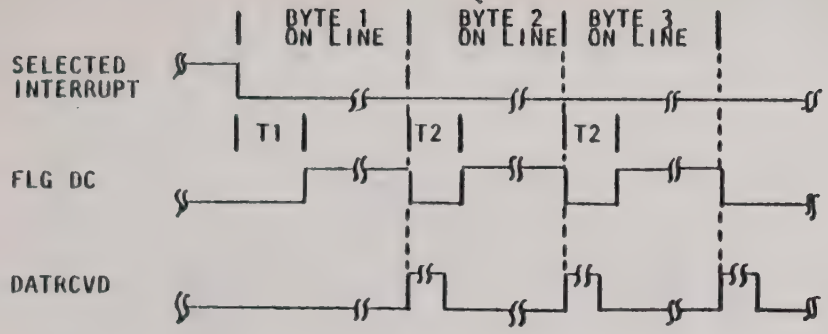
H.P. 12566B
TYPICAL TIMING RELATIONSHIPS
FIGURE 1



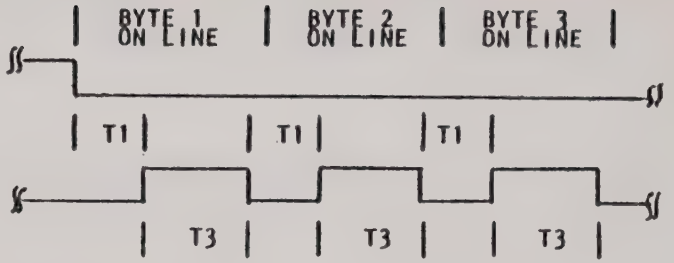
DEMAND/RESPONSE

T--Approximately 3 Microseconds

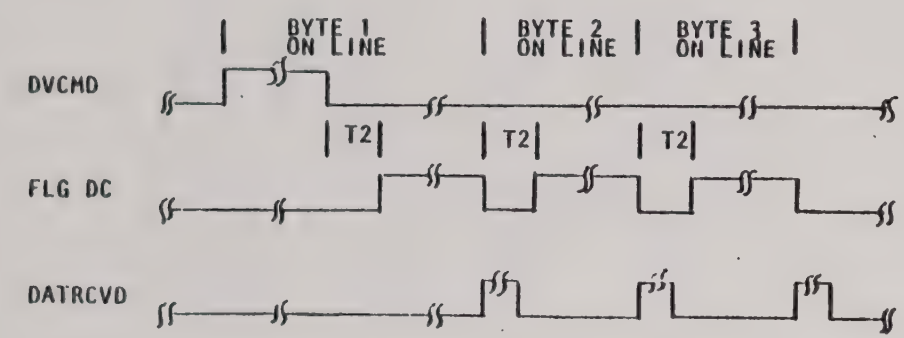
DEC DR11C
TYPICAL TIMING RELATIONSHIPS
FIGURE 2



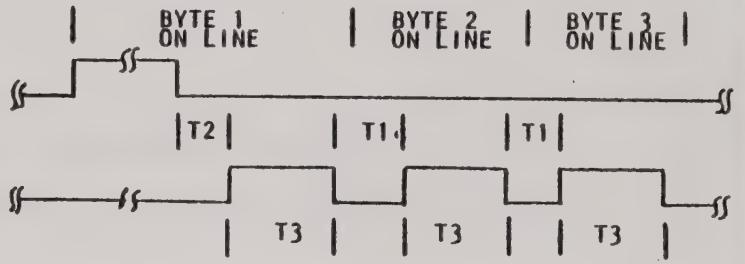
SELECTED TIME INTERRUPT SEQUENCE



SELECTED TIME AUTOMATIC SEQUENCE



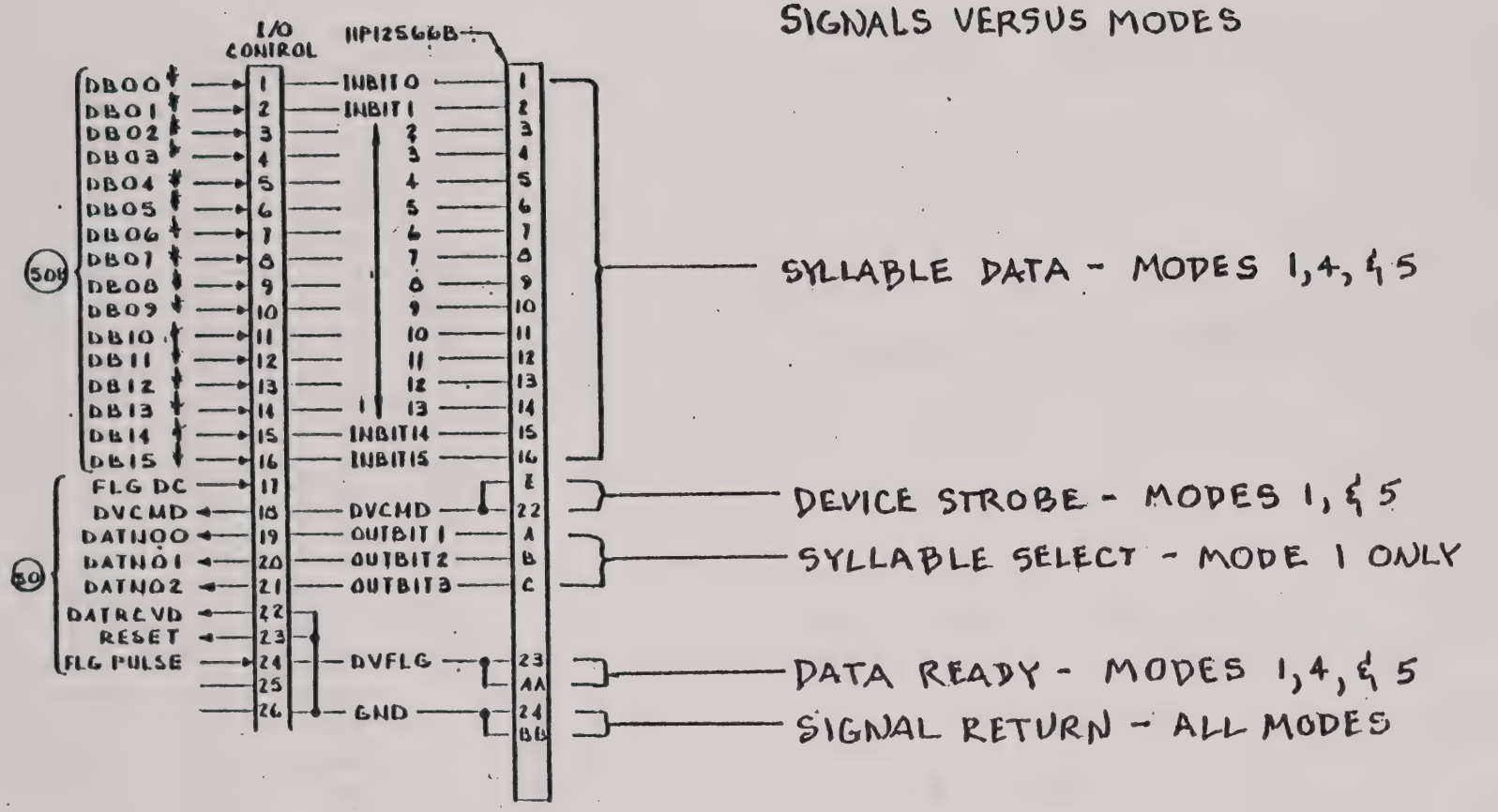
DEMAND TIME INTERRUPT SEQUENCE



DEMAND TIME AUTOMATIC SEQUENCE

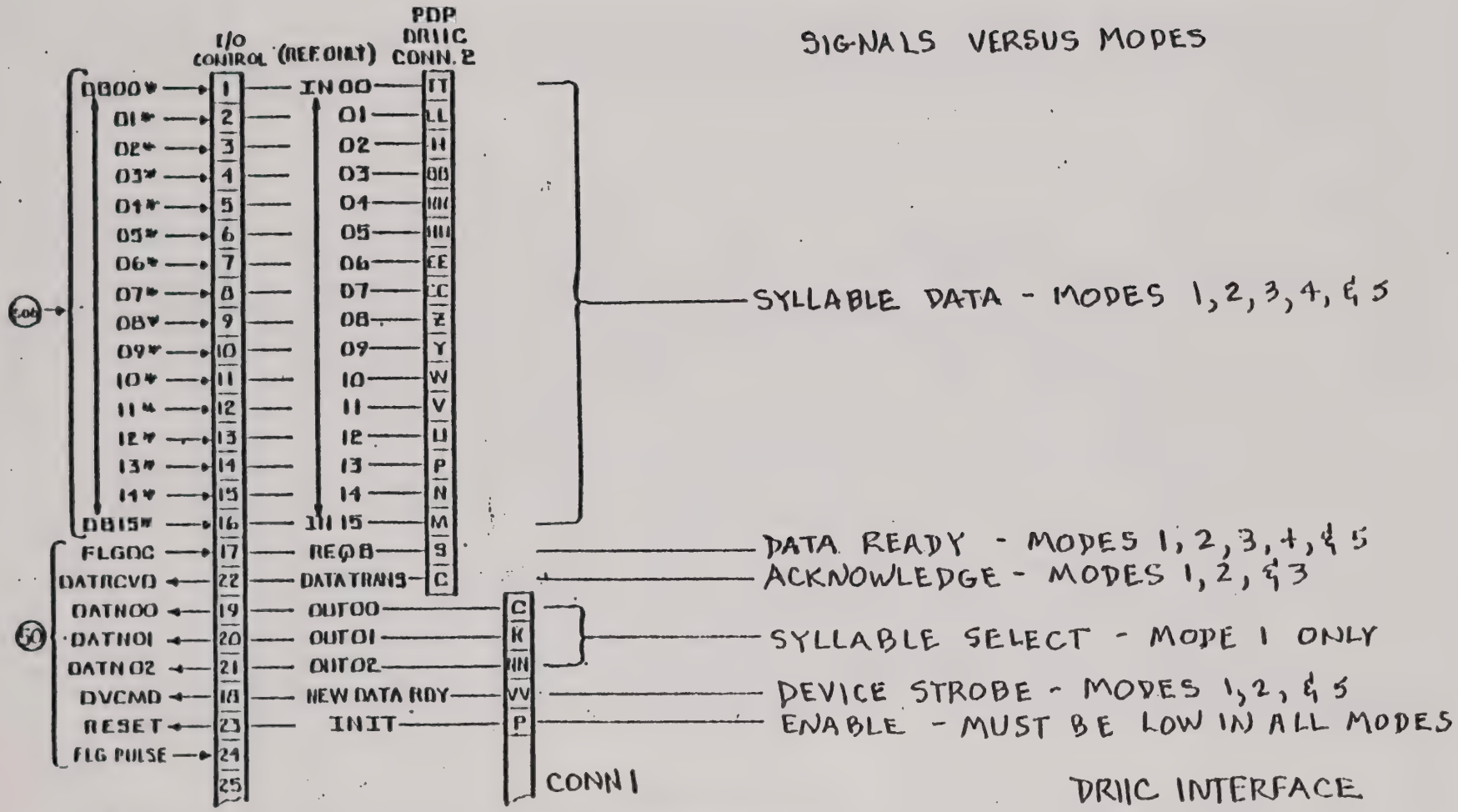
T1--Approximately 4 Microseconds
T2--Approximately 3 Microseconds
T3--Approximately 6 Microseconds

DEC DR11C
TYPICAL TIMING RELATIONSHIPS
FIGURE 3



SIGNALS VERSUS MODES

HP12566B INTERFACE
WIRING DIAGRAM



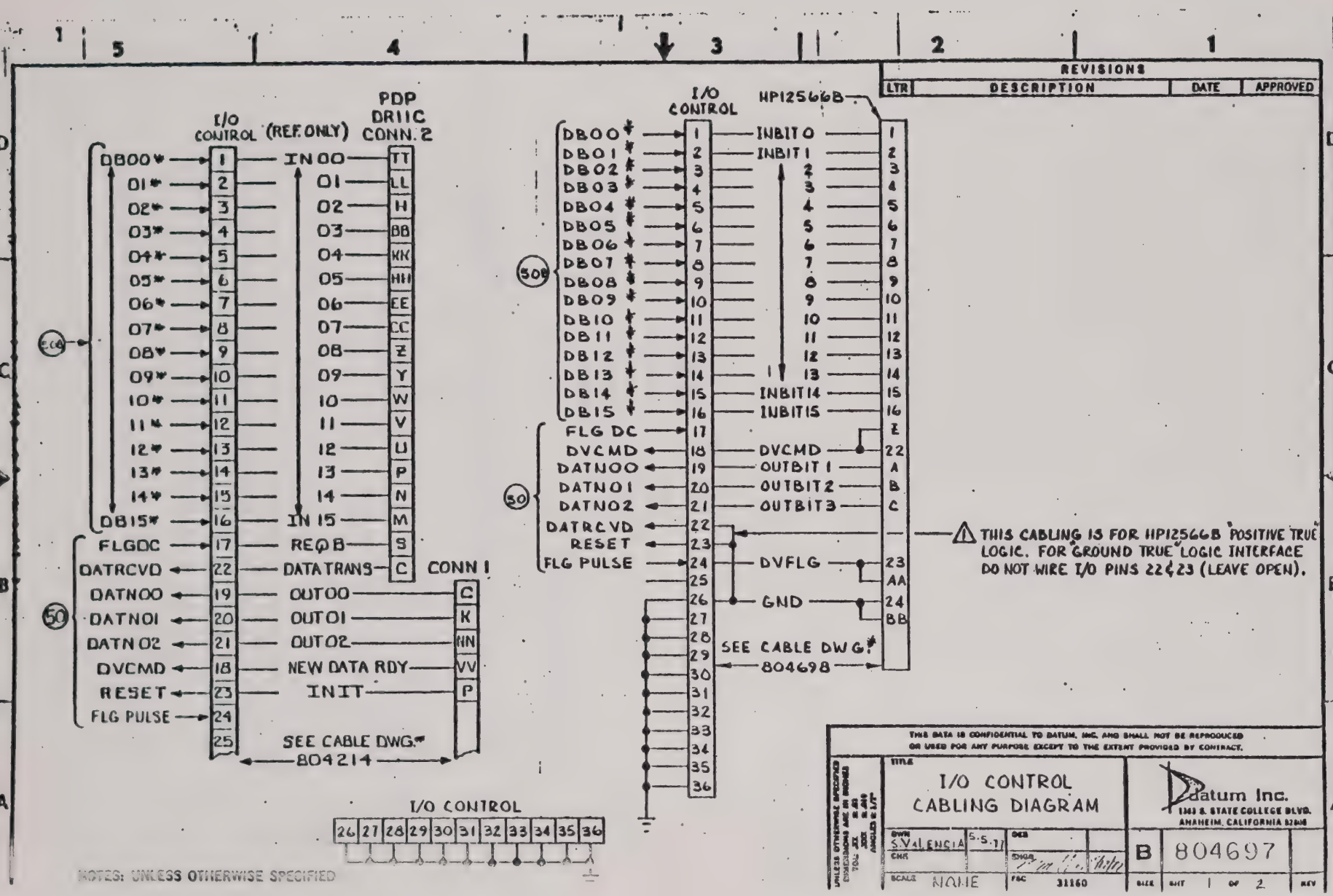
SIGNALS VERSUS MODES

DR11C INTERFACE WIRING DIAGRAM

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT NUMBER
																WORD 0
HOURS		MINUTES							SECONDS							WORD 1
UNITS		TENS			UNITS				TENS			UNITS				
2	1	4	2	1	8	4	2	1	4	2	1	8	4	2	1	
DAYS												HOURS				WORD 2
HUNDREDS				TENS				UNITS				TENS		UNITS		
8	4	2	1	8	4	2	1	8	4	2	1	2	1	8	4	
		INPUT LOSS*	BIT ERROR*	MILLISECONDS												WORD 3
				HUNDREDS				TENS				UNITS				
				8	4	2	1	8	4	2	1	8	4	2	1	
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT NUMBER

* STATUS BITS (IF AVAILABLE)

OUTPUT DATA FORMAT



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.

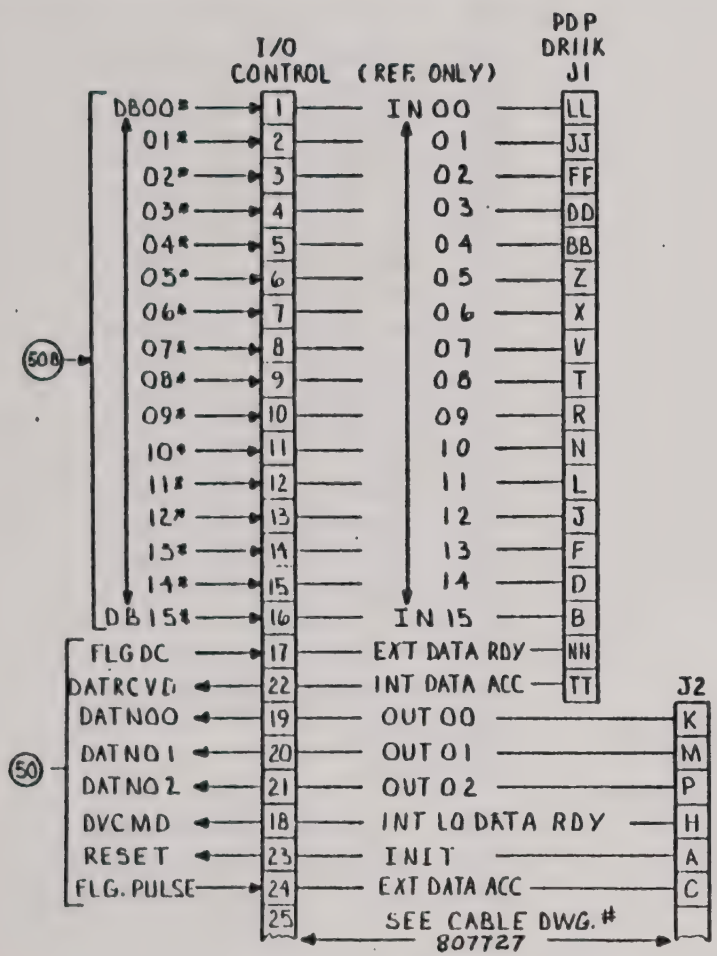
TITLE: I/O CONTROL CABLING DIAGRAM

Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

DWN SVALENSIA 5-5-77 | CHK | ENGR | MFG | SCALE NONE | FSC 31160

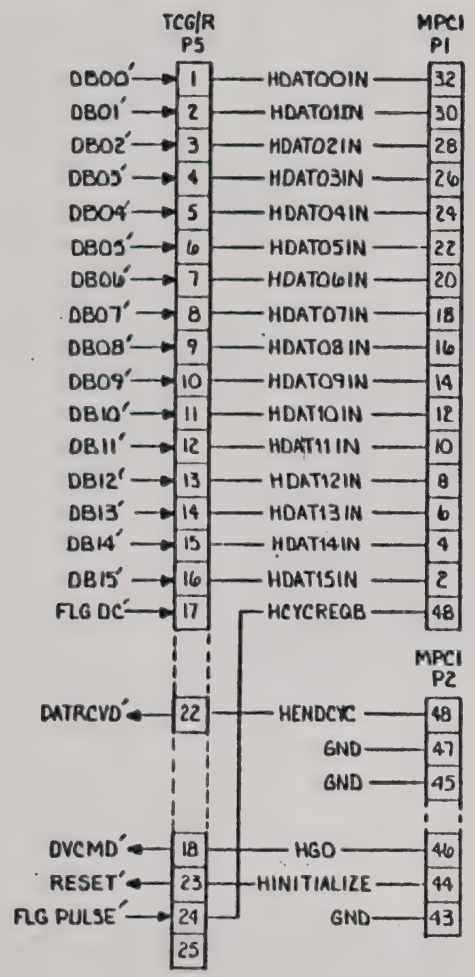
B 804697

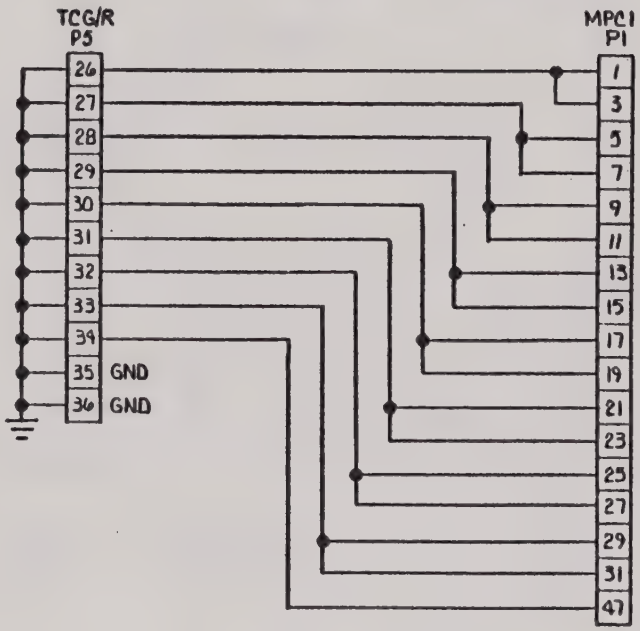
SIZE | SHT 1 OF 2 | REV

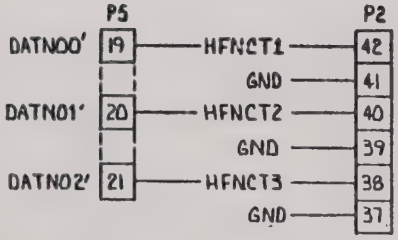

I/O CONTROL
(REF. ONLY)
PDP DRIIK J1
DB00* 1 IN 00 LL
01* 2 01 JJ
02* 3 02 FF
03* 4 03 DD
04* 5 04 BB
05* 6 05 Z
06* 7 06 X
07* 8 07 V
08* 9 08 T
09* 10 09 R
10* 11 10 N
11* 12 11 L
12* 13 12 J
13* 14 13 F
14* 15 14 D
DB15* 16 IN 15 B
50
FLG DC 17 EXT DATA RDY NN
DATRCVD 22 INT DATA ACC TT
J2
DATNO0 19 OUT 00 K
DATNO1 20 OUT 01 M
DATNO2 21 OUT 02 P
DVC MD 18 INT LQ DATA RDY H
RESET 23 INIT A
FLG. PULSE 24 EXT DATA ACC C
25
SEE CABLE DWG. # 807727
I/O CONTROL
26 27 28 29 30 31 32 33 34 35 36

I/O CONTROL CABLING DIAGRAM	B	804697	
THIS DATA IS CONFIDENTIAL TO DATUM, INC. AND SHALL NOT BE REPRODUCED OR USED FOR ANY PURPOSE EXCEPT TO THE EXTENT PROVIDED BY CONTRACT.	SIZE	SHT 2 OF 2	REV

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED







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TITLE
CABLING DIAGRAM (SEL MPCI 8020 INTERFACE)

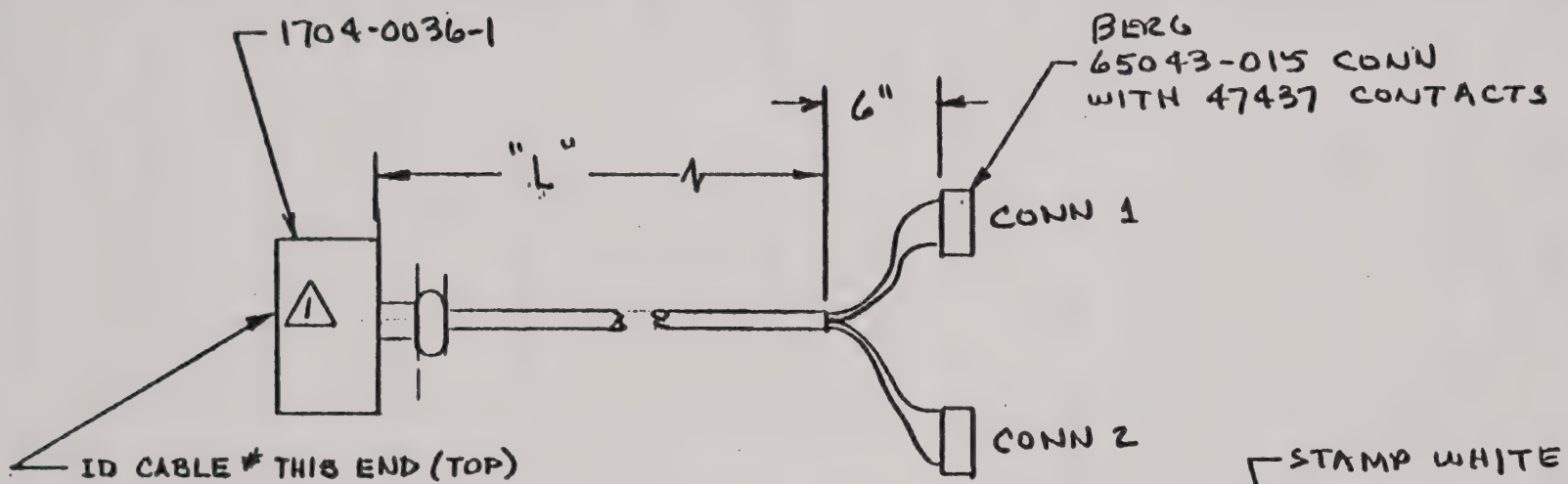
datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

DWN	TERI	11/15/83	DES			
CHK			ENGR			
SCALE	NONE		FSC	31260	SIZE B	SHT 1 OF 1 REV

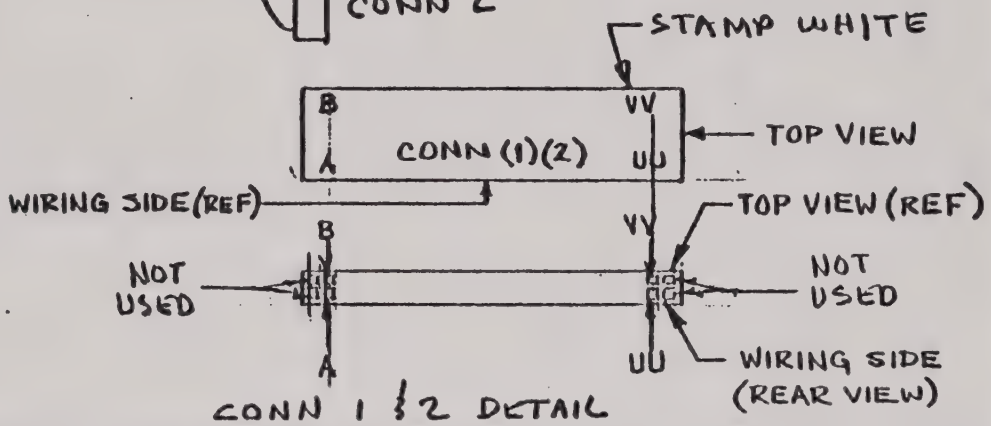
809253

NOTES: UNLESS OTHERWISE SPECIFIED

LTR	DESCRIPTION	DATE	APPROVED



-08	8 FT
-25	25 FT
-10	10 FT
-40	40 FT
DASH NO	"L"



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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: .XX ± .03
.XXX ± .010
ANGLES ± 1/2°

TITLE: CABLE (DRIIC INTERFACE)

DWN R Plank 4/24/96		DES	
CHK		ENGR	
SCALE NONE		FSC 81160	

Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

SIZE		SHT	REV
A	804214	1 OF 2	

1 FOR RCA ONLY, SEE ATTACHED SPECIFICATION ON259715

NOTES: UNLESS OTHERWISE SPECIFIED

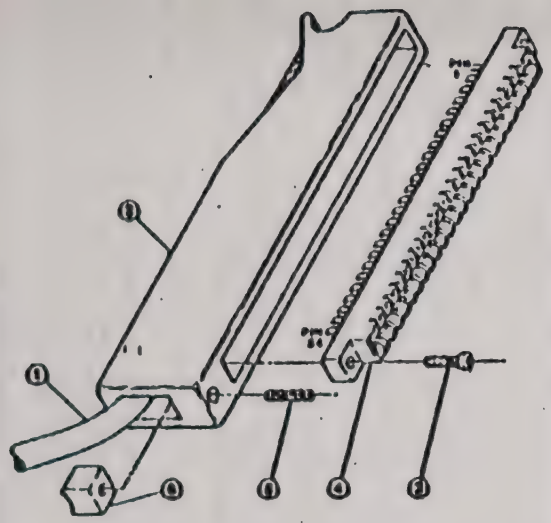
FROM		TO		FROM		TO	
J5 - 19		CONN 1 - C	OUT00	J5 - 1		CONN 2 - TT	IN 00
↑ - 35	*	↑ - J	GND	↑ - 26	*	* ↑ - UU	GND
| - 20		- K	OUT01	- 2		- LL	IN 01
| - 35	*	- M	GND	- 26	*	* - UU	GND
| - 21		- NN	OUT02	- 3		- H	IN 02
| - 36	*	- MM	GND	- 27	*	* - R	GND
| - 18		- VV	NEW DATA RDY	- 4		- BB	IN 03
| - 36	*	- UU	GND	- 27	*	* - AA	GND
↓ - 23		- P	INIT	- 5		- KK	IN 04
J5 - 36	*	CONN 1 - S	GND	- 28	*	* - JJ	GND
				- 6		- HH	IN 05
				- 28	*	* - JJ	GND
				- 7		- EE	IN 06
				- 29	*	* - AA	GND
				- 8		- CC	IN 07
				- 29	*	* - DD	GND
				- 9		- Z	IN 08
				- 30	*	* - DD	GND
				- 10		- Y	IN 09
				- 30	*	* - PP	GND
				- 11		- W	IN 10
				- 31	*	* - X	GND
				- 12		- V	IN 11
				- 31	*	* - X	GND
				- 13		- U	IN 12
				- 32	*	* - T	GND
				- 14		- P	IN 13
				- 32	*	* - R	GND
				- 15		- N	IN 14
				- 33	*	* - L	GND
				- 16		- M	IN 15
				- 33	*	* - L	GND
				- 17		- S	REQ B
				- 34	*	* - T	GND
				- 22		- C	DATA TRANS
				J5 - 34	*	*CONN 2-PP	GND

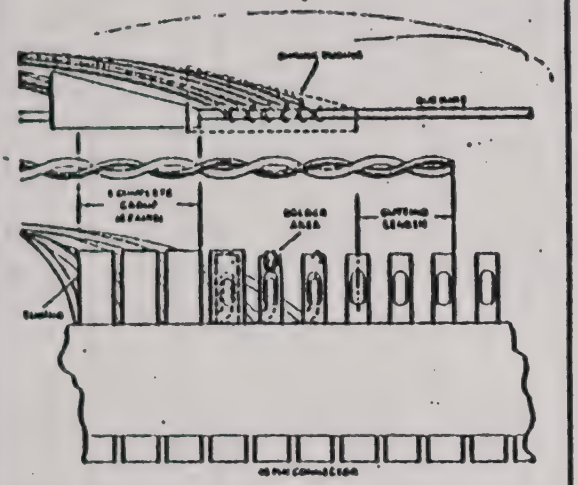
DWG. NO. 804214 REV.

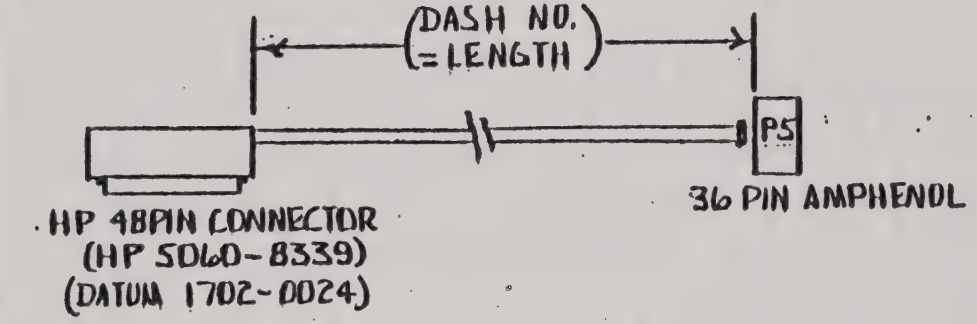
Datum inc.

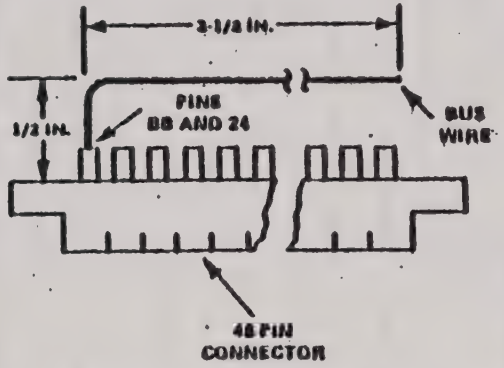
*indicates 2 wires per pin (J5 - 36 has 3 wires).

LTR	DESCRIPTION	DATE	APPROVED









EXAMPLE	
-NO	LENGTH
-50	= 50 FEET

ITEM	DESCRIPTION	PART NO.
1	Cable, 38 twisted pair	8120-1846 or equivalent
2	Connector hood	5040-6071
3	Self-tapping screw	0624-0098
4	Connector, 48 pin	1251-0335
5	Setscrew	3030-0143
6	Cable clamp	5040-6003

NOTES: UNLESS OTHERWISE SPECIFIED

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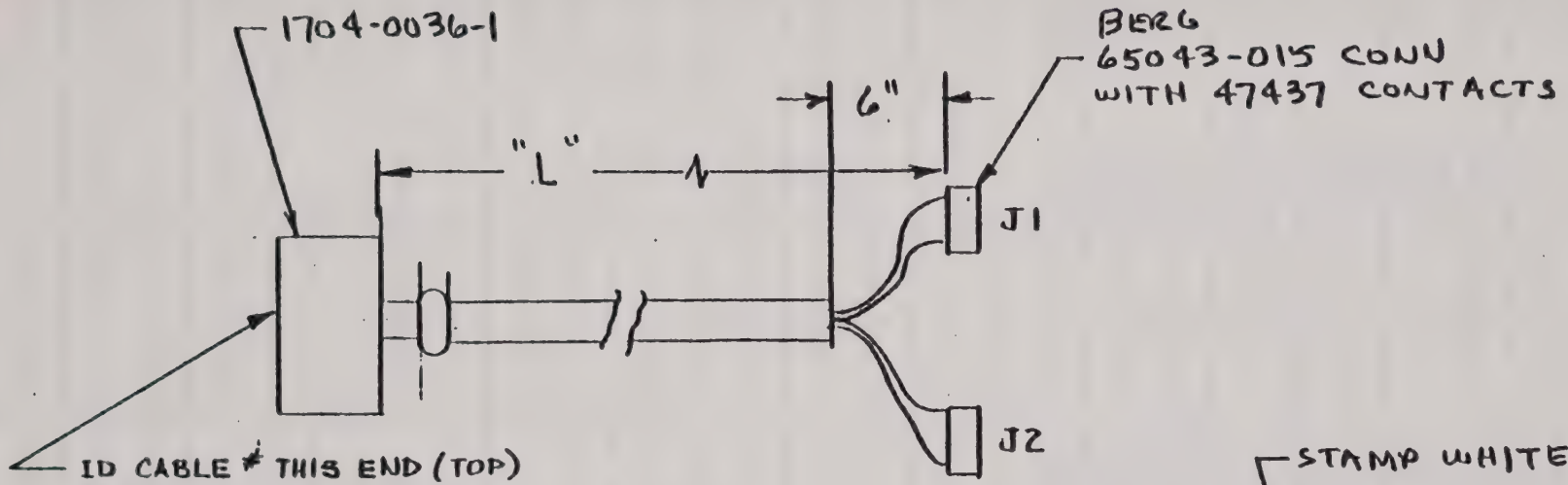
TITLE: CABLE TO HP 1251-0335

DWN: [signature] 5/6/11 | DES | CHK | ENGR | SCALE | FSC 81160

datum inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

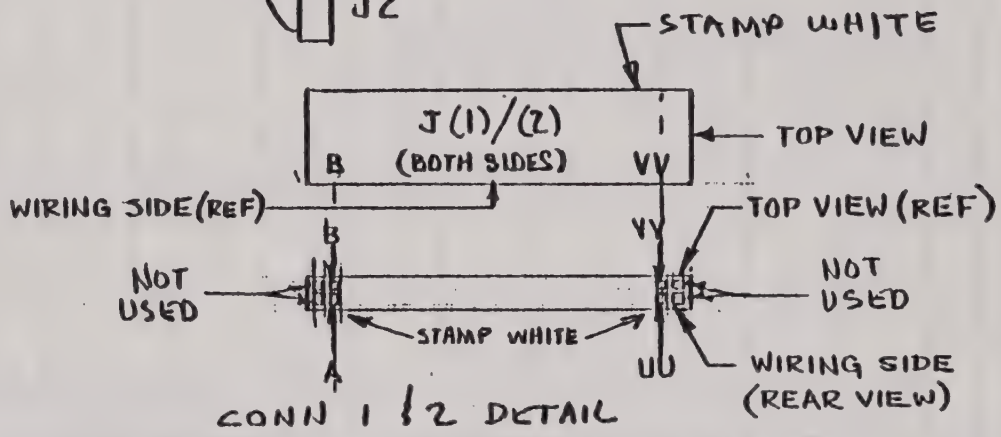
A | B0469B | SIZE | SHT 1 OF 2 | REV

FROM		TO	SIGNAL	FROM		TO	SIGNAL
J5 - 1		HP - 1	D800	J5 - 18		22, 3	DVCMD
⚠ - 26		(GNDBUS)*	RET	⚠ - 34		(GNDBUS)*	RET
| - 2		- 2	D801	| - 19		- A	DATNO0
| - 26		*	RET	| - 35		*	RET
| - 3		- 3	D802	| - 20		- B	DATNO1
| - 27		*	RET	| - 35		*	RET
| - 4		- 4	D803	| - 21		- C	DATNO2
| - 27		*	RET	| - 36		(GNDBUS)*	RET
| - 5		- 5	D804	↓ - 22	GND		
| - 28		*	RET	J5 - 23	GND		
| - 6		- 6	D805				
| - 28		*	RET				
| - 7		- 7	D806				
| - 29		*	RET				
| - 8		- 8	D807				
| - 29		*	RET				
| - 9		- 9	D808				
| - 30		*	RET				
| - 10		- 10	D809				
| - 30		*	RET				
| - 11		- 11	D810				
| - 31		*	RET				
| - 12		- 12	D811				
| - 31		*	RET				
| - 13		- 13	D812				
| - 32		*	RET				
| - 14		- 14	D813				
| - 32		*	RET				
| - 15		- 15	D814				
| - 33		*	RET				
| - 16		- 16	D815				
| - 33		*	RET				
↓ - 24		↓ 23, AA	FLG.PULSE				
J5 - 24		(GNDBUS)*	RET				



TYPICAL

-08	8 FT
-25	25 FT
-10	10 FT
-40	40 FT
DASH NO	"L"



CONN 1 & 2 DETAIL

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOL: XX ± .03
XXX ± .010
ANGLES ± 1/2°

TITLE: CABLE (DRIIK INTERFACE)

DWN		DES	
CHK		ENGR	1/80
SCALE NONE		FSC 81160	

Datum Inc.
1363 S. STATE COLLEGE BLVD.
ANAHEIM, CALIFORNIA 92806

SIZE	DWG NO	REV
A	BD7727	
	SHT 1 OF 2	

NOTES: UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS / ACCURITE®

FROM		TO		FROM		TO	
J5 - 19		J2 - K	OUT00	J5- 1		J1 - LL	IN 00
-35	*	- L	GND	- 26	*	- MM	GND
-20		- M	OUT01	- 2		- JJ	IN 01
-35	*	- N	GND	- 26	*	-KK	GND
-21		- P	OUT02	- 3		-FF	IN 02
-36	*	- R	GND	- 27	*	-HH	GND
-18		- H	Lo Data RDY	- 4		-DD	IN 03
-36	*	- J	GND	- 27	*	-EE	GND
-23		- A	INIT	- 5		-BB	IN 04
-36	*	- B	GND	- 28	*	-CC	GND
-24		- C	EXT DATA ACC	- 6		-Z	IN 05
J5 -35	*	J2 - D	GND	- 28	*	-AA	GND
				- 7		-X	IN 06
				- 29	*	-Y	GND
				- 8		-V	IN 07
				- 29	*	-W	GND
				- 9		-T	IN 08
				- 30	*	-U	GND
				- 10		-R	IN 09
				- 30	*	-S	GND
				- 11		-N	IN10
				- 31	*	-P	GND
				- 12		-L	IN 11
				- 31	*	-M	GND
				- 13		-J	IN 12
				- 32	*	-K	GND
				- 14		-F	IN 13
				- 32	*	-H	GND
				- 15		-D	IN 14
				- 33	*	-E	GND
				- 16		-B	IN 15
				- 33	*	-C	GND
				- 17		-NN	EXT DATA RDY
				- 34	*	-PP	GND
				- 22		-TT	INT DATA ACC
				J5 - 34	*	J1 - UU	GND

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DWG. NO. 807727 REV

PAGE 2 of 2

* Indicates 2 wires per pin (J5 -35 &36) has 3 wires).

APPENDIX B
OPTIONAL FEATURES

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